

GA-AX370-GAMING 5

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2015.12.30~B.L

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Title COVER SHEET			
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Model Name:GA-AX370-GAMING 5

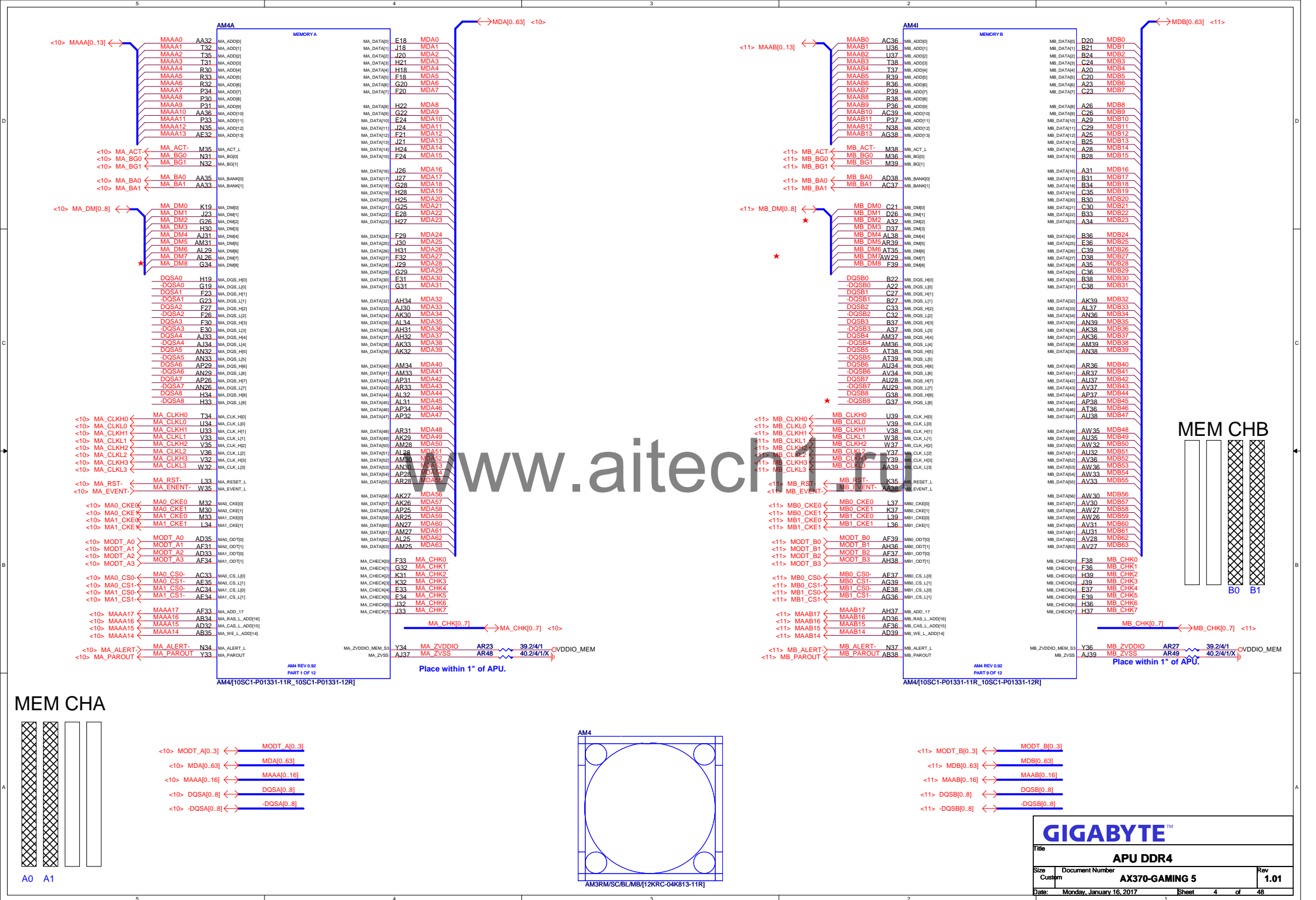
Component value change history

Version: 1.01
P-Code: U98126-0

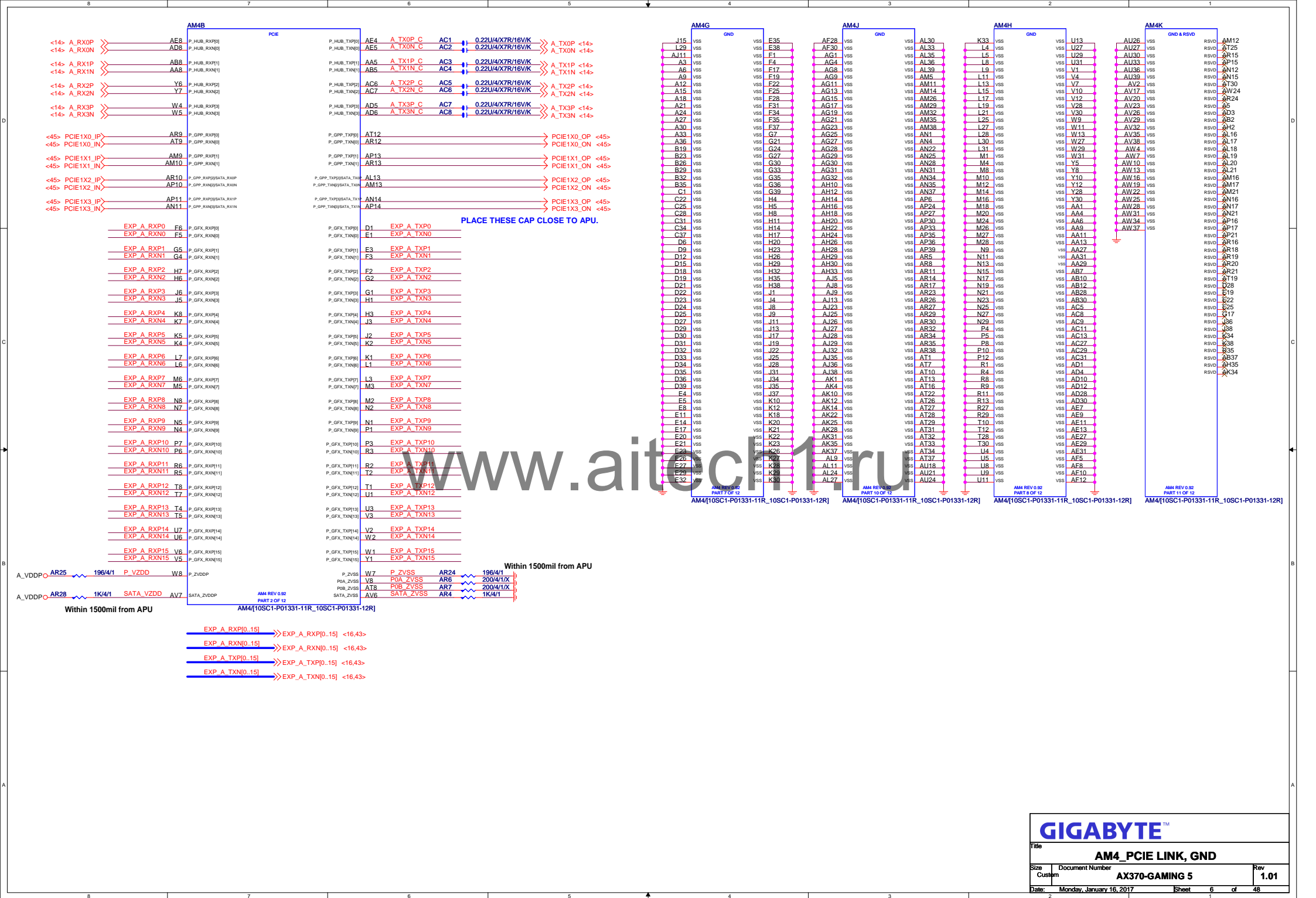
Date	Change Item	Reason
2016.08.08	01 New BOM Release. PCB: 0.1	1. OR169 NA 2. FIX PWM PHASE 6. 3. OR13, OR35 POP, OR33 NC. 4. AGPIO_4 add pull down. 5. FIX SATA_EXPRESS ISSUE. 6. USB SSC STRAP 7. DAC POWER P_EN-->P_GATE 8. PCIE Group 0/1 strap & sch 9. SATAExpress strap & sch 10. EFUSE_PWR SCH ADD 预留pull down sch 11. PAUC6/PAUC8 0402-->0603 10u 12. STARDUST MEASURE 13. DAR30&DAR27-->11K DAR61-->13K 14. PT USB30 Add Redriver 15. update codec 1220 VER:053 16. IT8686 ADD FOR FIX PSU VCC3 負壓 SCH 17. IT8792 BOM 18. WATCHDOG PIN CHANGE TO PIN47 & PIN90 19. DEBUG LED GPIO CHANGE TO SIO GP65 & GP95(CPU & DRAM LED) 20. PX2 FOOTPRINT CHANGE 21. ADD AR100 FOR O_-RTCRST 22. PR60/PR61 PULL UP, PR59/PR63 NA GPP GROUP0 23. PR22/PR65 PULL UP, PR64 NA GPP GROUP1 24. DDR SLOT "DDR4/288/BKVA/D/G15/TWO LATCH/SHELL"雙耳扣用料 25. MOS_T 12SP2-S09425-71R_12SP2-S09425-72R_12SP2-S09425-73R 26. MOD_R 12SP2-S08025-71R_12SP2-S08025-72R_12SP2-S08025-73R 27. USB31_LAN "11NR6-706009-51R"
2016.11.29	01 New BOM Release. PCB: 0.1	0. rename AX370-Gaming 5 1. OR37 PULL 3VDUAL_IO(部分SIO POWER改接3VDUAL_IO for ERP) 2. BEEP- 原GP27 改接 GP15 (IT8686 Pin32), OR26 Pull hi 刪除 3. MB_ID2 原GP26 改接 GP65 (IT8686 Pin82), 4. TPM PIN1 修改,不接SIO,改接至CPU 5. LPC from EC8792 (注意FW) 6. MR19 N/A, MR0 上件, OR38 / OR39 上件 (Debug LED) 7. OC Botton GPIO CHANGE 8. DUAL BIOS from EC8792(須注意FW) 9. CC change to TI3220 10. PCH_TEMP/X16_TEMP/X16_TEMP2 change to 10K/4/1/S 11. FPQ351/FPQ80/FPQ81 先不上件 12. MOS_T/R & PCH HS 料號修改 13. MA_DR12 2K-->1.91K
2017.01.16	101 New BOM Release. PCB: 101	1. MASK XMP & TURBO 2. ECR100 PULL TO VCC3 3. CPU_FAN color CHANGE TO GRAY 4. DAU1 Update PN:10TA1-635201-08R 5. FPQ351 上件 For Watchdog 6. ECR21 NA (預防AGPIO85誤動作) 7. PR7 change to 10p, PC15/PC16 NA 8. OR51 CHANGE TO 0ohm NA 9. PT Crystal 1M-->10p / 匹配cap NA

Circuit or PCB layout change for next version

Date	Change Item	Reason
2017.01.13	Rev 1.01 Gerber-out	1. MASK XMP & TURBO 2. ECR100 PULL TO VCC3 3. PUMP1/2 change name SYS_FAN5_PUMP,SYS_FAN6_PUMP, 4. SIO & EC 48M ADD OR1 & ECR30 1K PULL DOWN

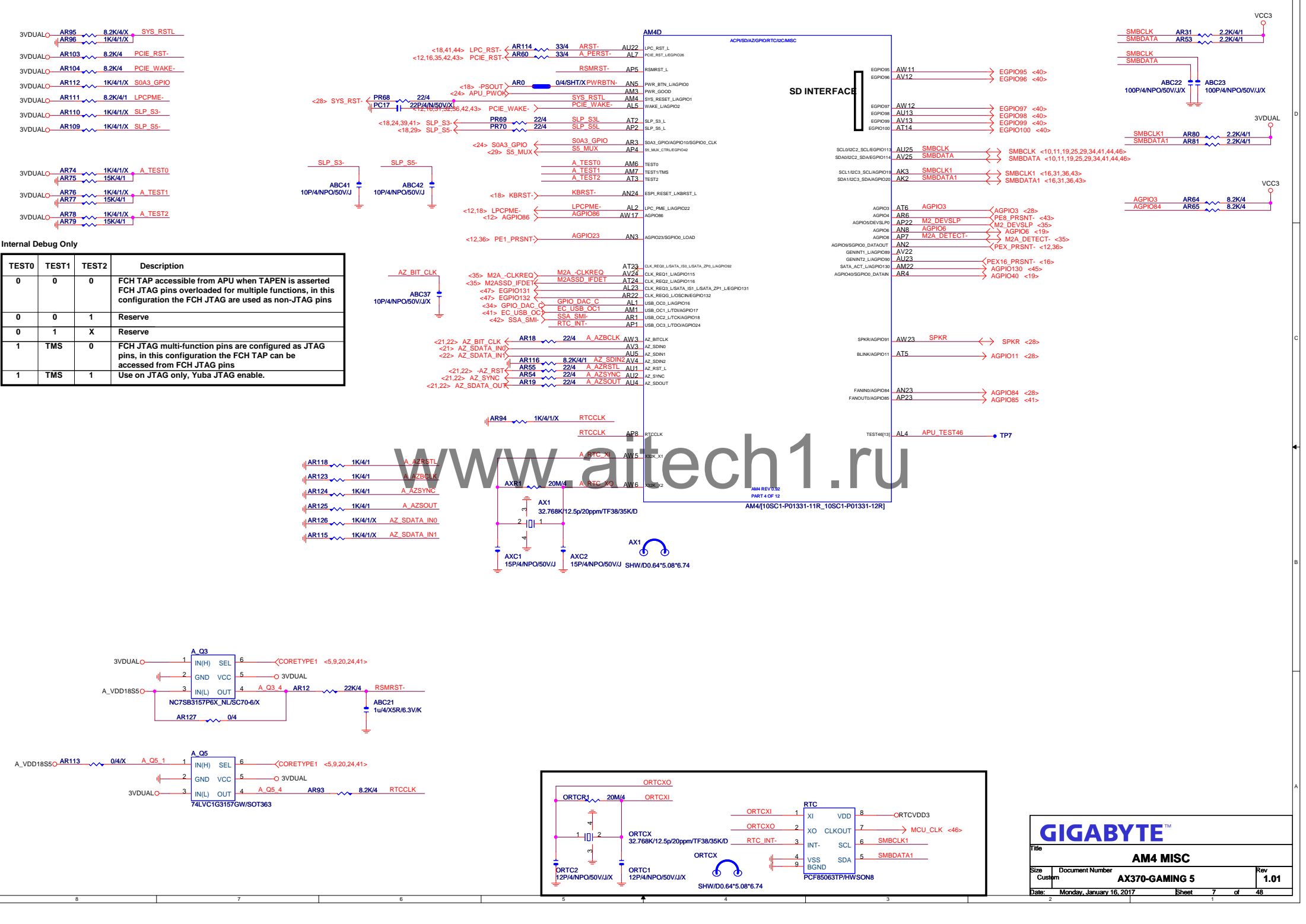






Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



GIGABYTETM

Title

AM4 MISC

Size

Document Number

Rev

Custom

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1.01

Date

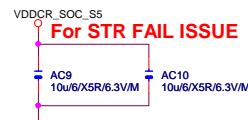
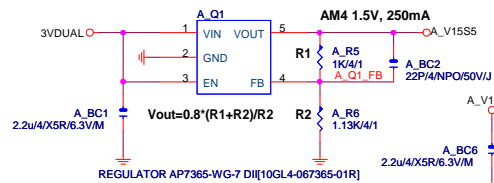
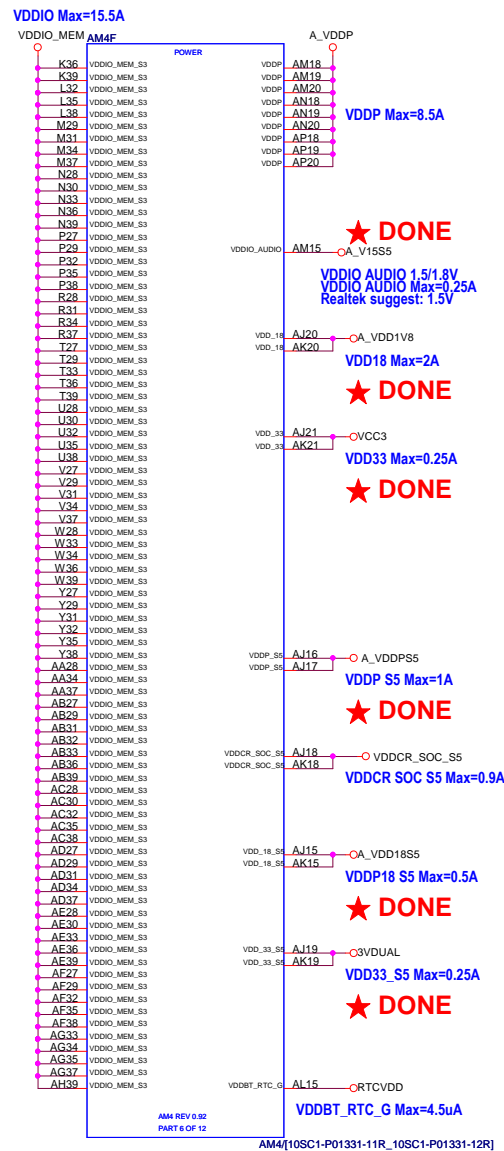
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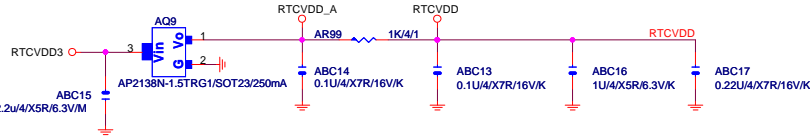
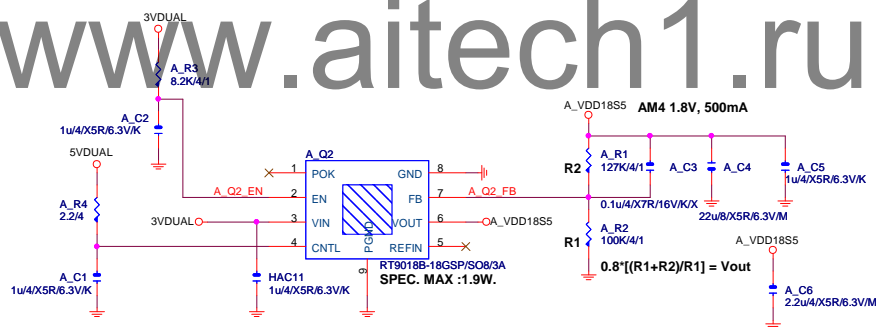
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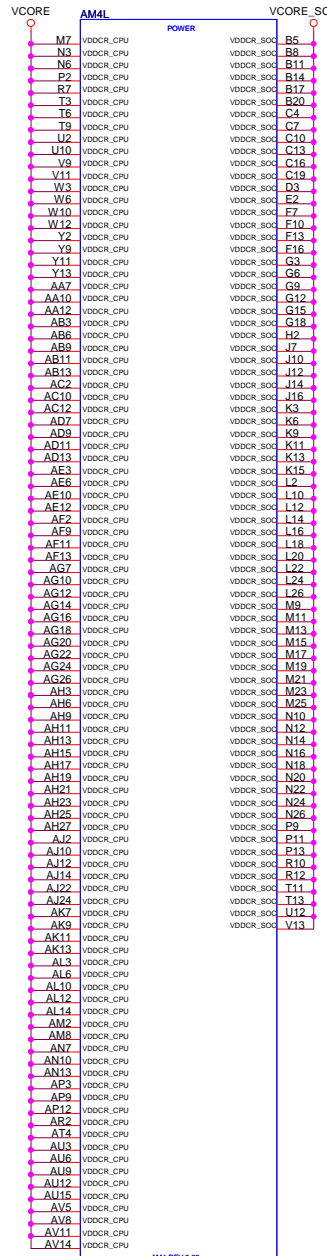
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CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

Vcore EDC=75A
Vcore 0.75-1.5V

Vcore SOC EDC=75A
Vcore SOC 0.75-1.2V



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Title

CPU POWER & GND

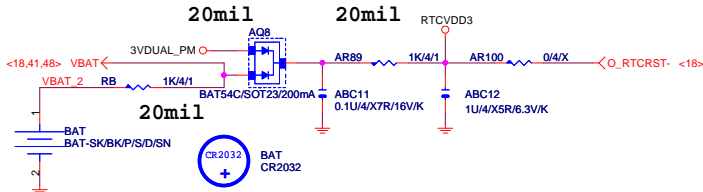
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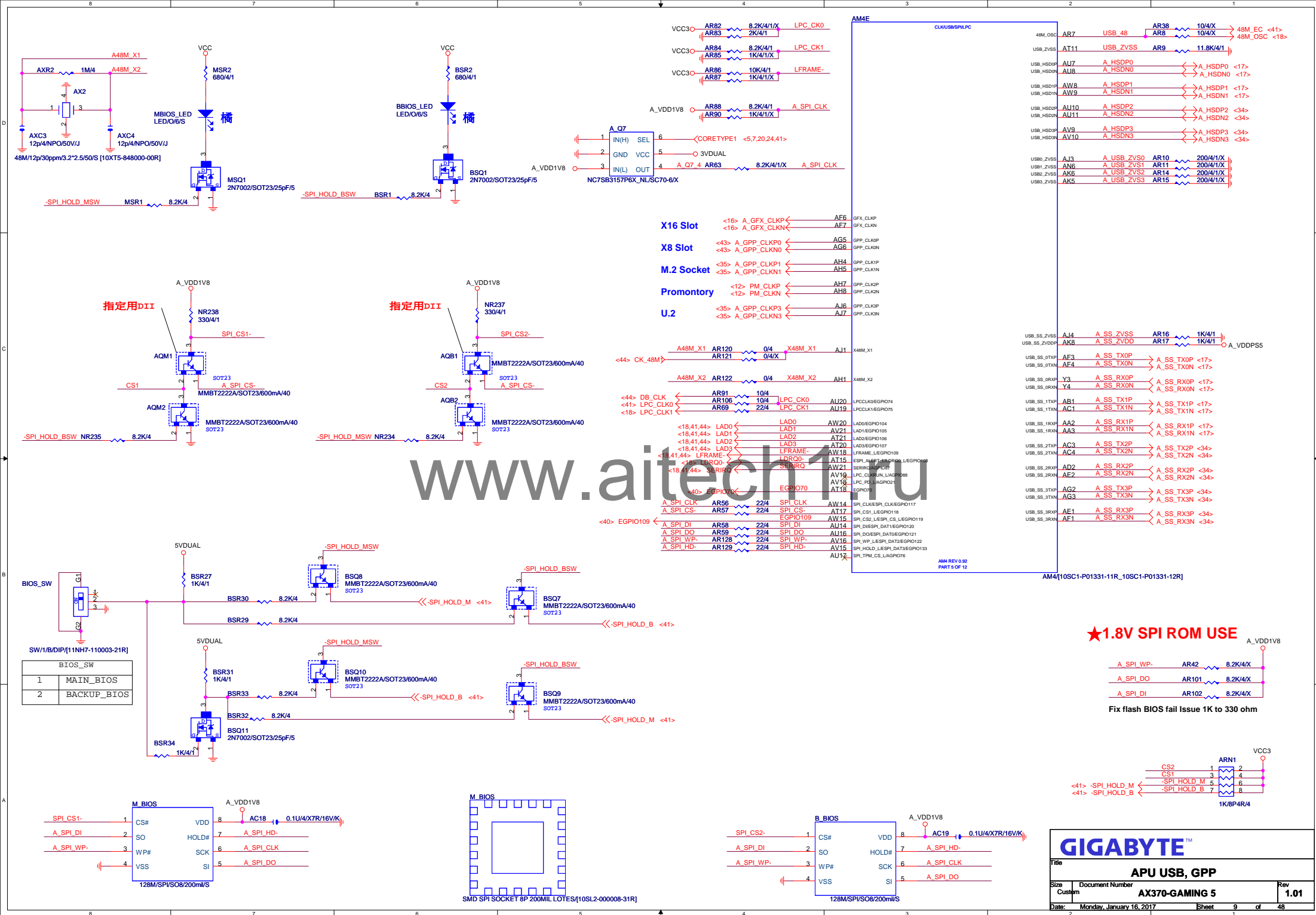
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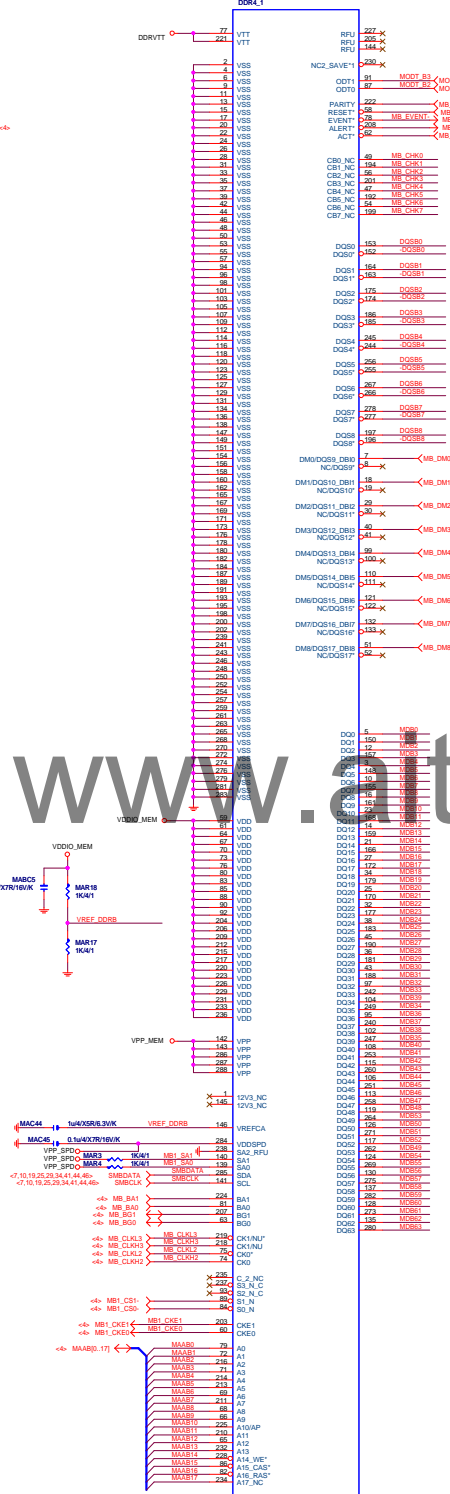








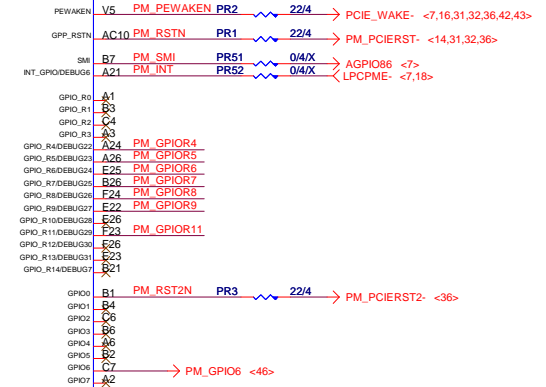
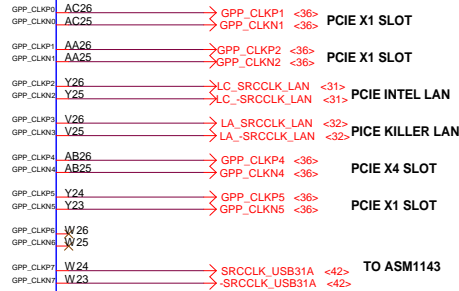
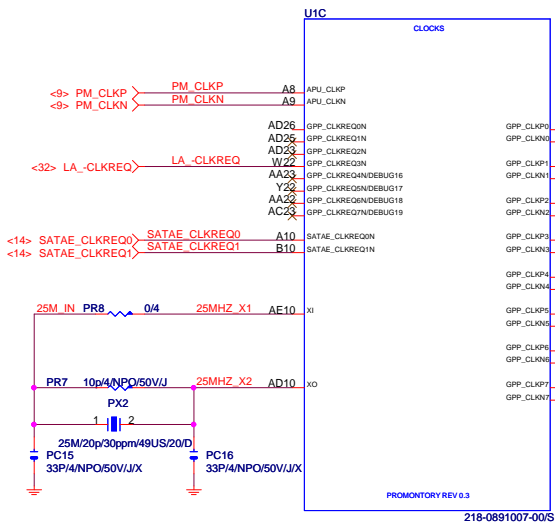
CHANNEL B0
SA2:1=001



CHANNEL B1
SA2:3=011

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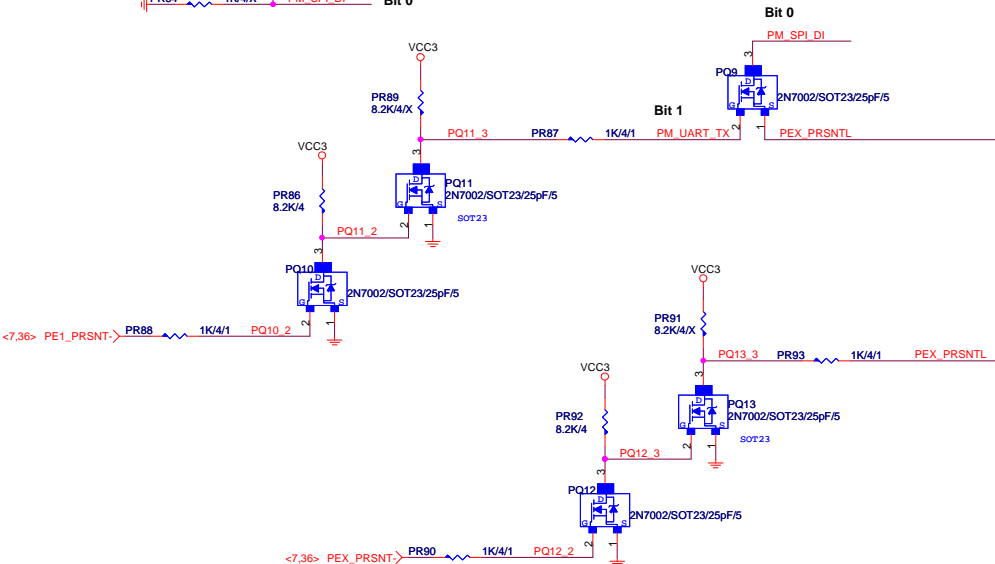
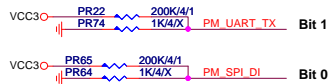
GIGABYTE		
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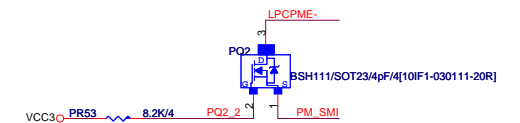
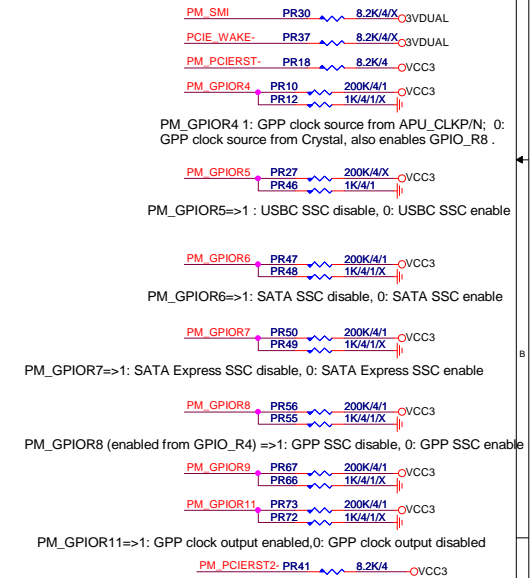
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PM GPP Group 0=>0-3



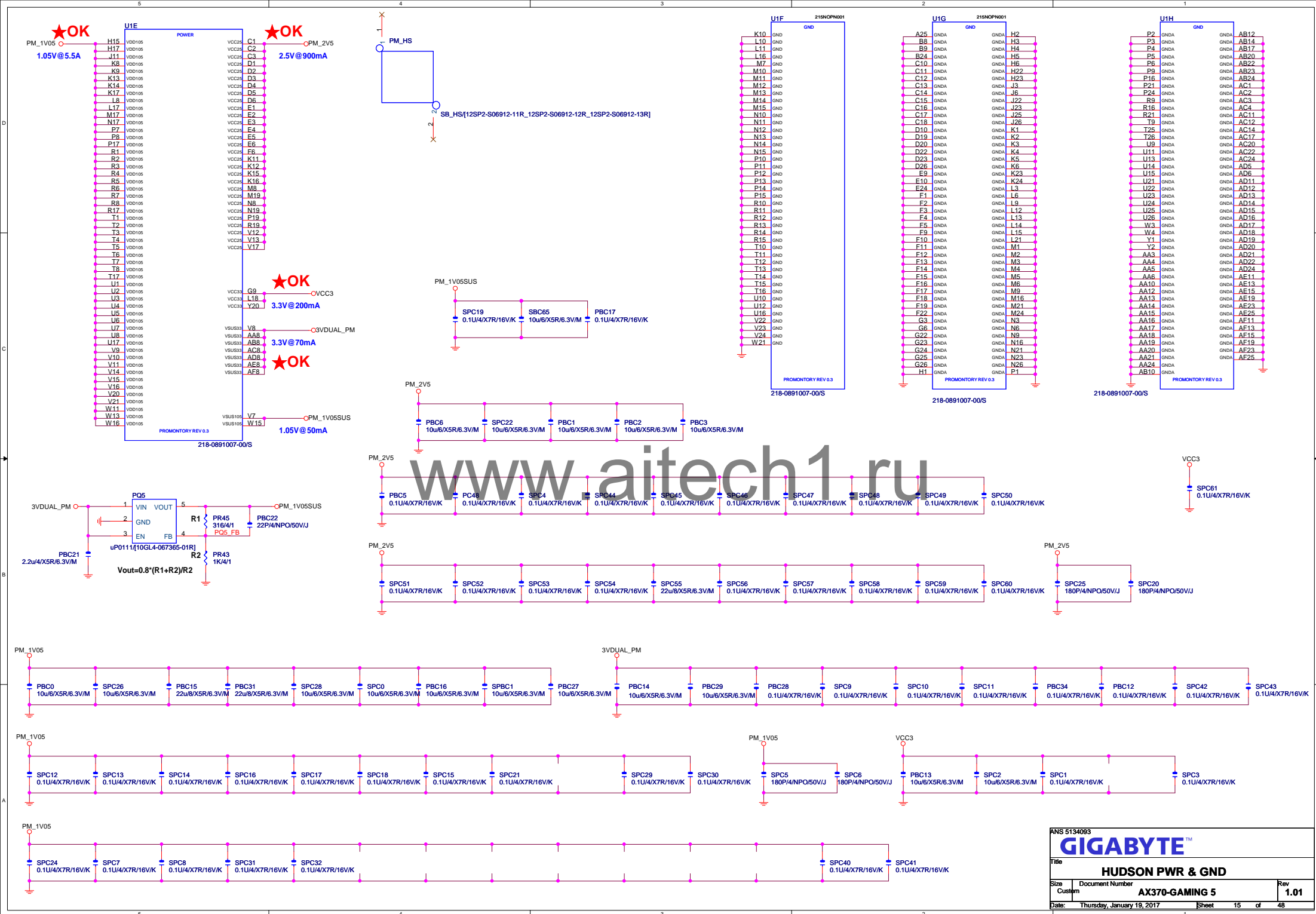
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PM GPP Group 1=>4-7

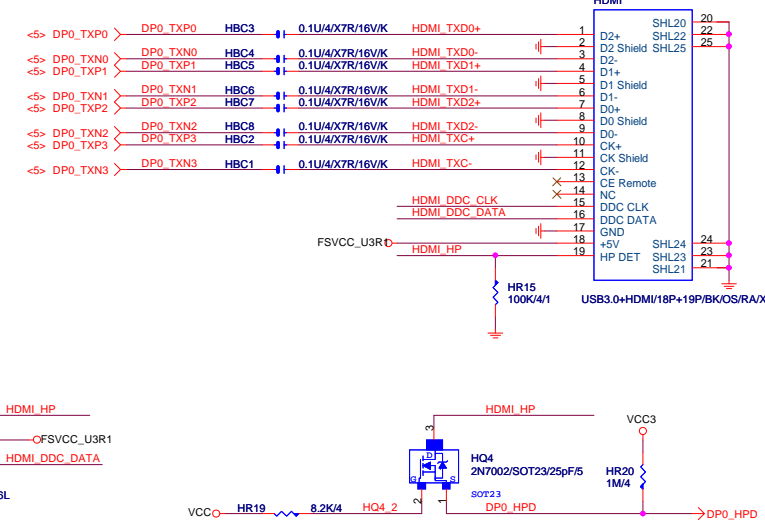
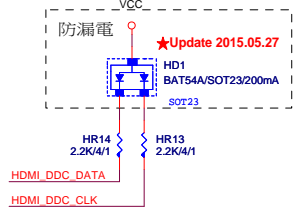
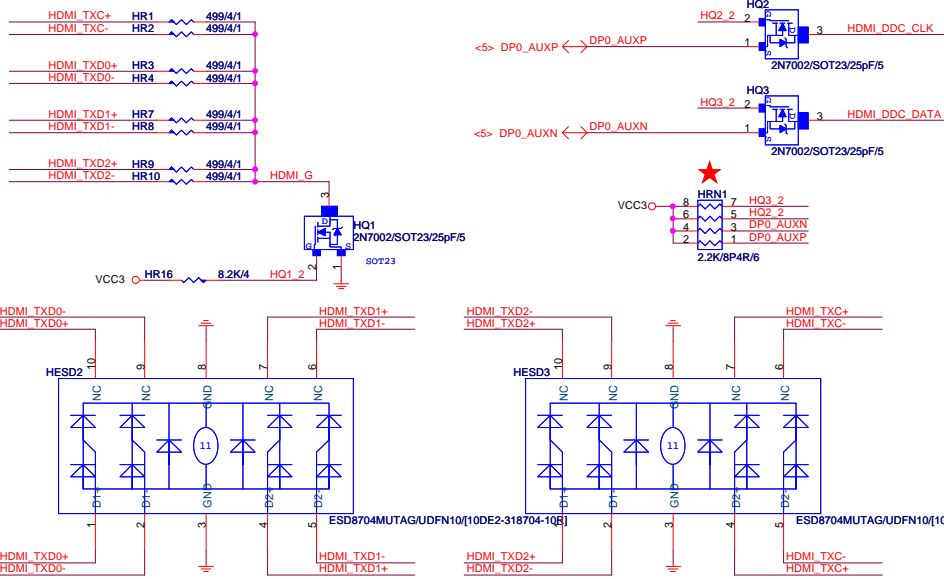


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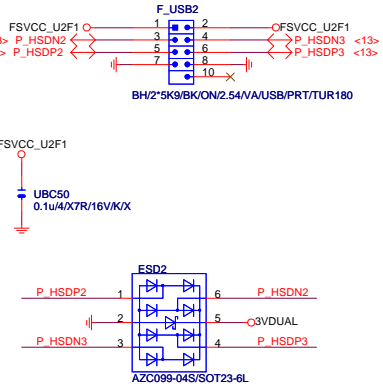


ANS 5134063			
GIGABYTE			
Title			
PROMONTORY CPU/CLK/MISC			
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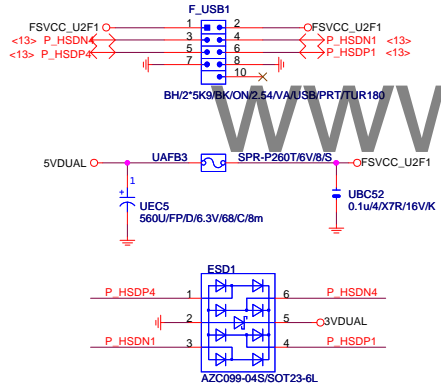




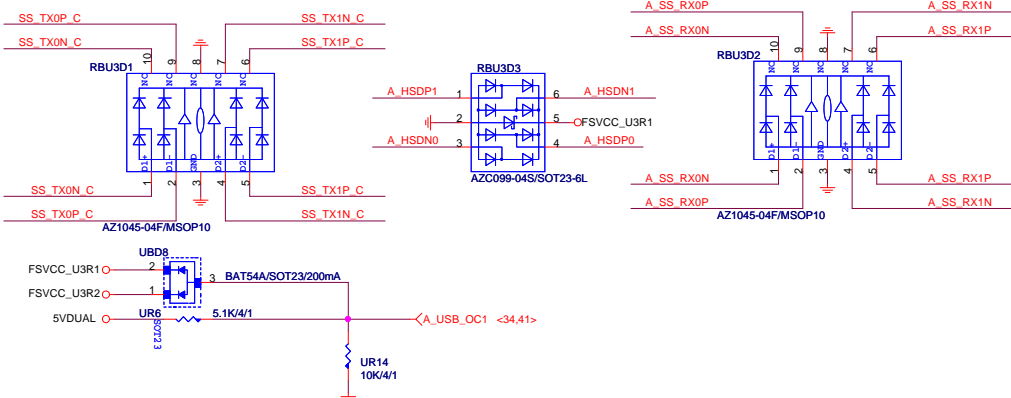
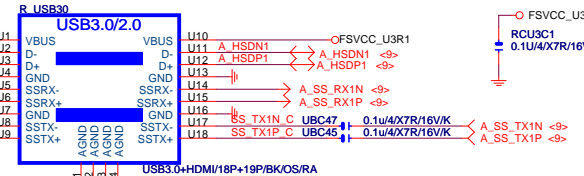
FRONT SIDE USB2

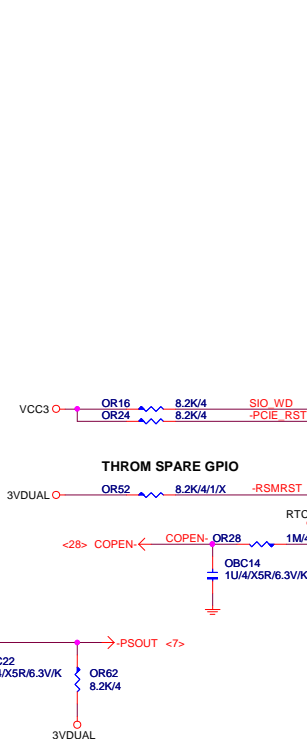


FRONT SIDE USB1



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SIO STRAP

OR33 1K/4/I JP2 OR36 8.2K/I4 VCC3
 OR81 1K/4/I/X JP3 OR35 8.2K/4/X 3VDUAL_I/O
 OR80 1K/4/I/X JP4 OR32 8.2K/4 3VDUAL_I/O
 JP5 OR12 8.2K/4 3VDUAL_I/O
 JP7 OR37 8.2K/4 3VDUAL_I/O

			
Title ITE 8686 LPC IO, TPM, KB/MS			
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SIO PU

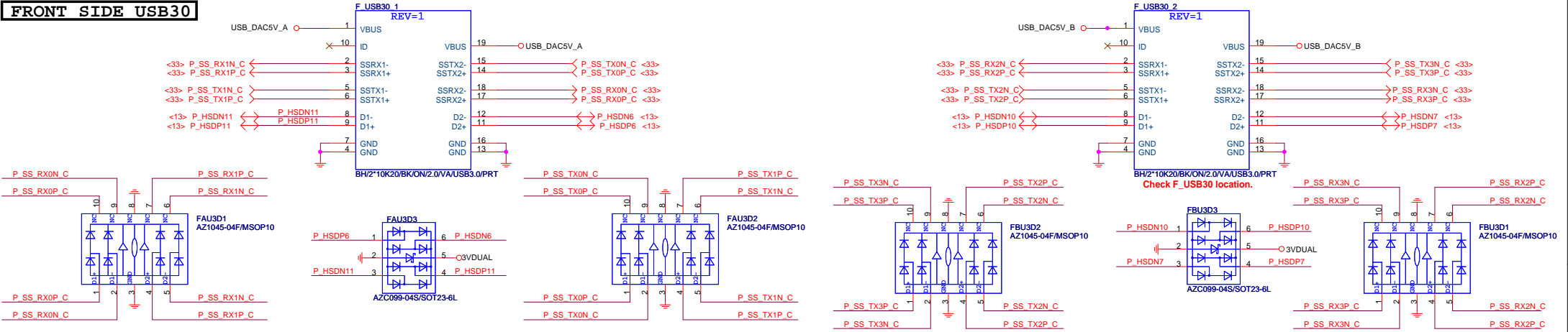
LDRQ0- OR27 1K/4/1 VCC3

PRST1- OR11 1K/4/1 VCC3

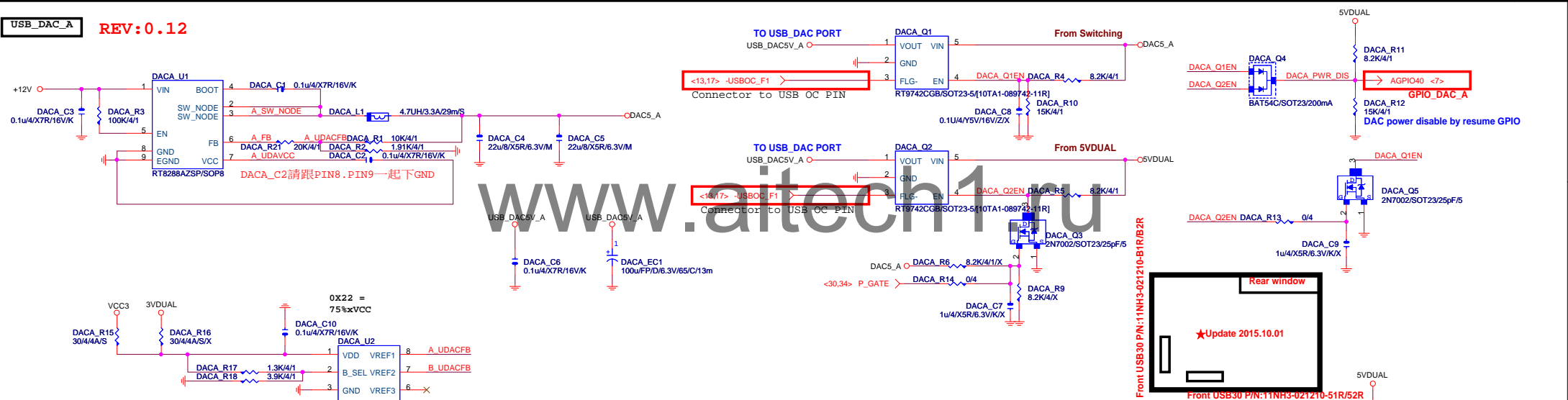
ITE_PWROK OR10 1K/4/1 VCC3

CLOSE SIO PIN4 2_5LEVEL

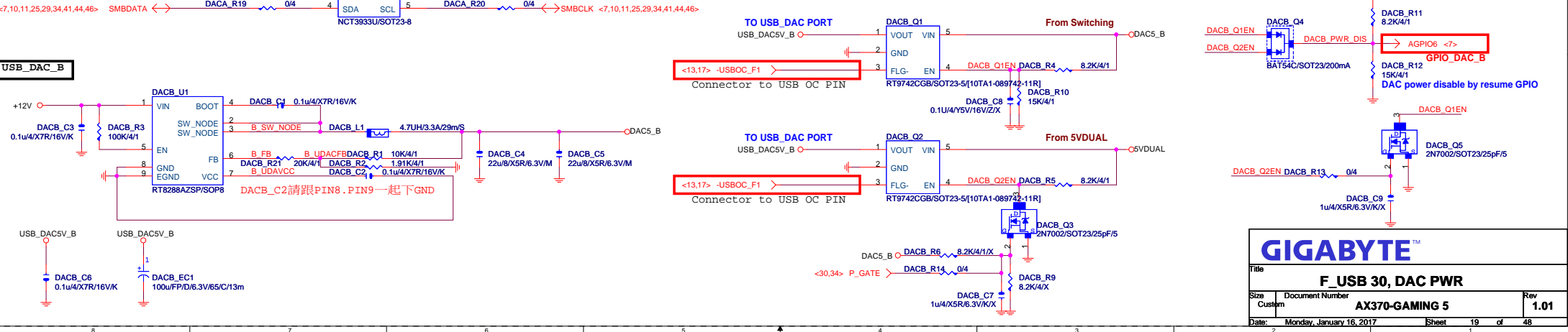
FRONT SIDE USB30



USB_DAC_A REV:0.12

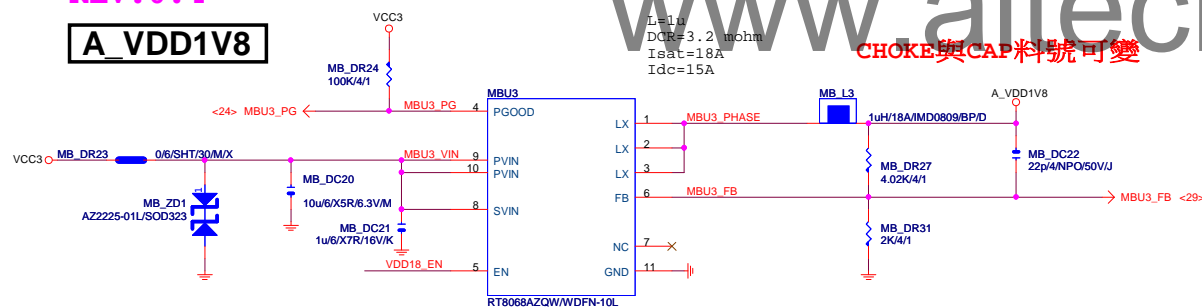


USB_DAC_B



REV:0.4

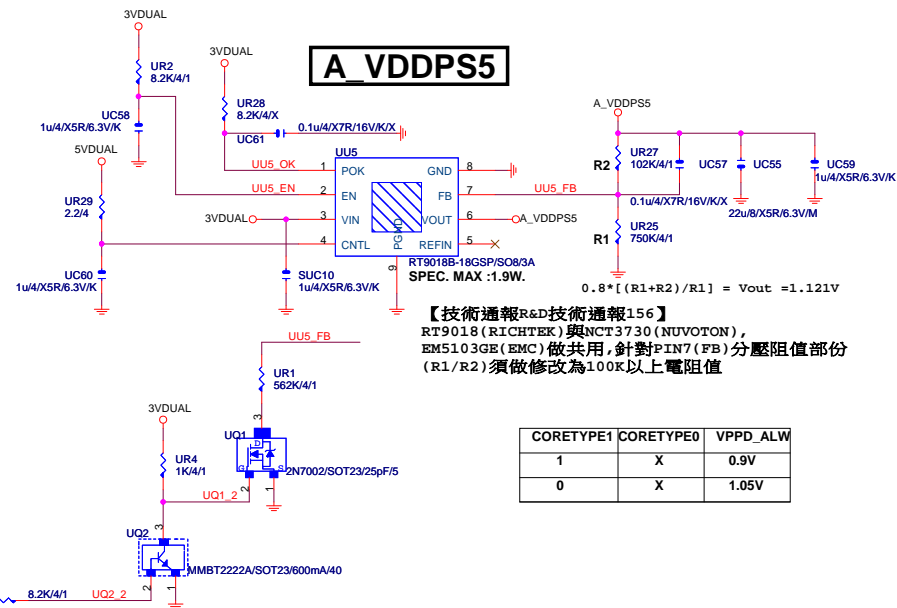
A_VDD1V8



L=1uH
DCR=3.2 mOhm
I_{sat}=18A
I_{dc}=15A

CHOKE與CAP料號可變

A_VDDPS5



【技術通報R&D技術通報156】
RT9018 (RICHTER)與NCT3730 (NUVOTON),
EM5103GE (EMC)做共用,針對PIN7 (FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值

$$0.8 * [(R1+R2)/R1] = V_{out} = 1.121V$$

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

VPP CAP

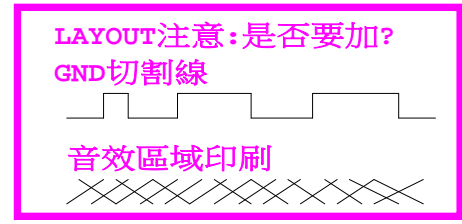
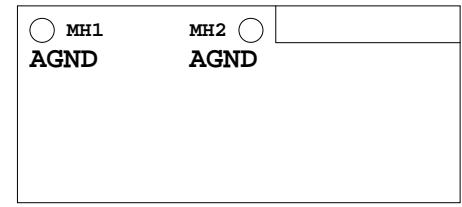
* 大電容 >0

22u*1PCS

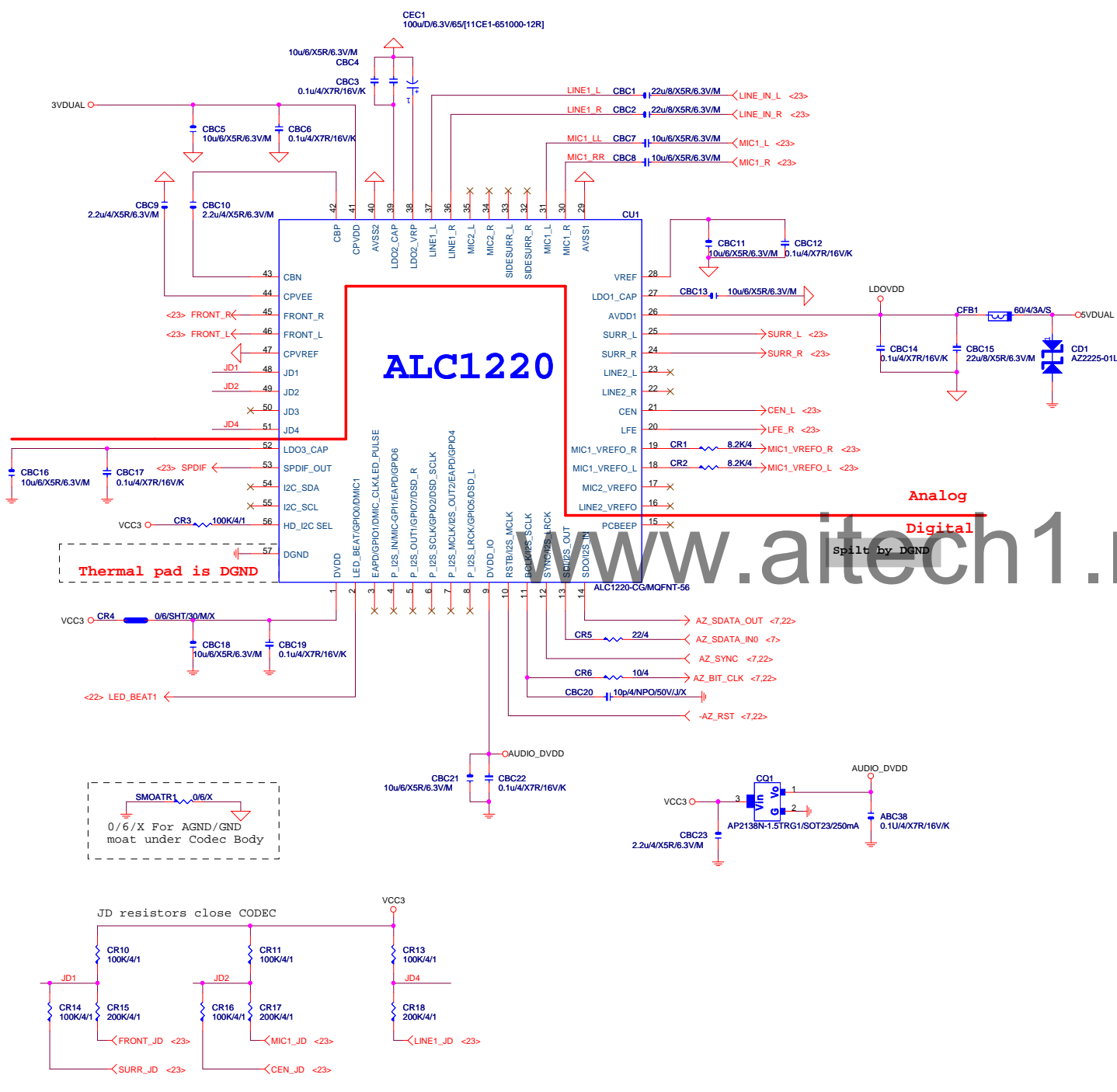
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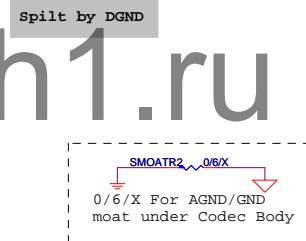
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LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,改為Isolate
2. MH2一律改為Isolate

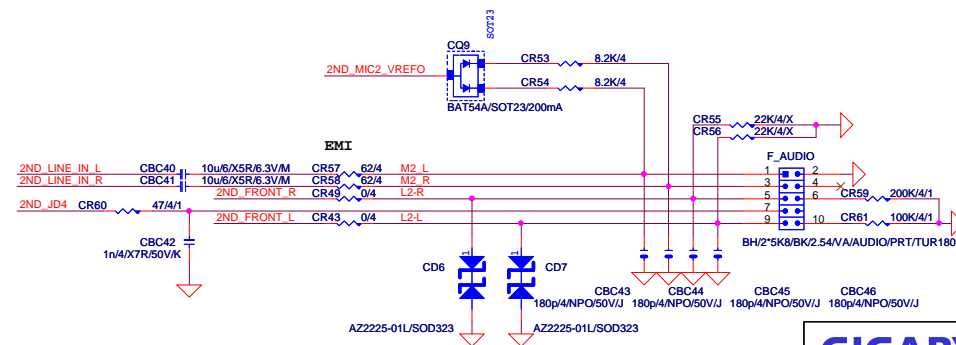


BOM OPTION :
1. AUDIO CONNECT
不銹鋼料號:11NR6-403025-A2R
鍍金料號:11NR6-403025-92R
2. AUDIO CAP
Nichicon MW音效電容 : 11CE1-651000-12R
Chemicon音效電容 : 11CE2-651000-05R



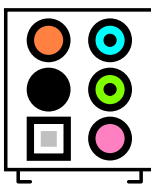


AZALIA FRONT PANEL

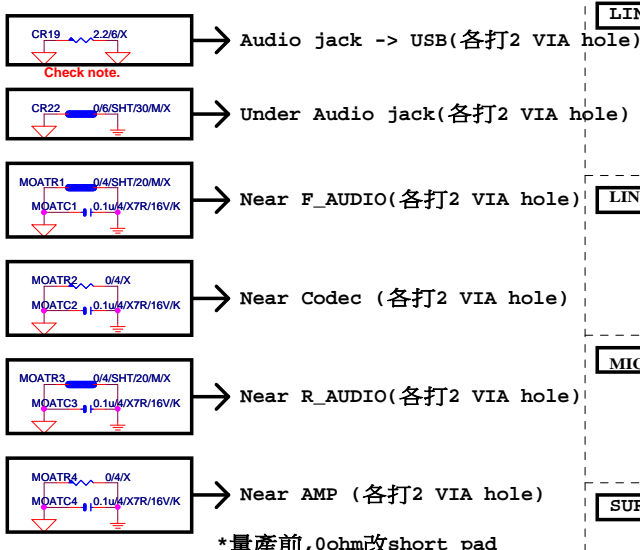
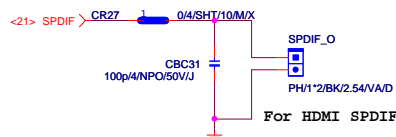


Rev 0.1

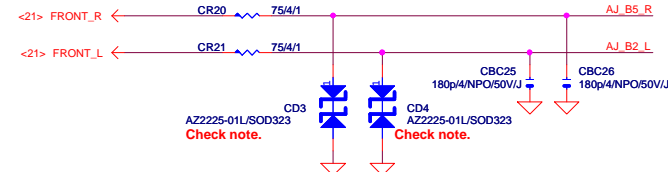
AZALIA JACK



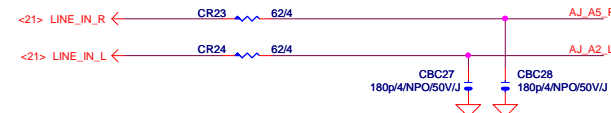
SPDIF_OUT



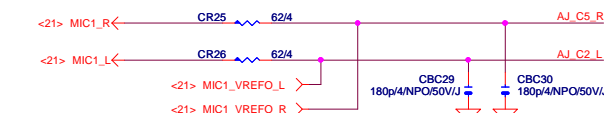
LINE-OUT



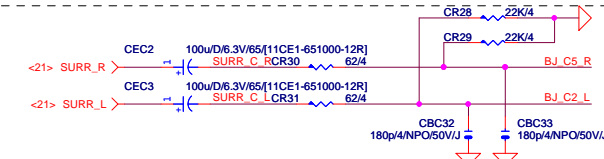
LINE-IN



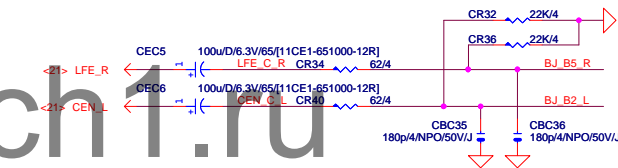
MIC-IN



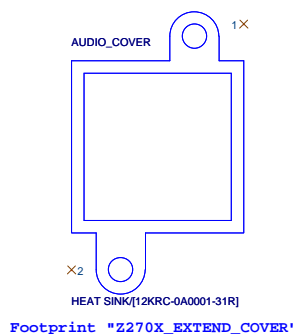
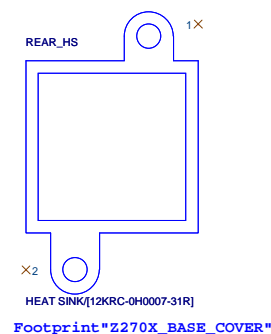
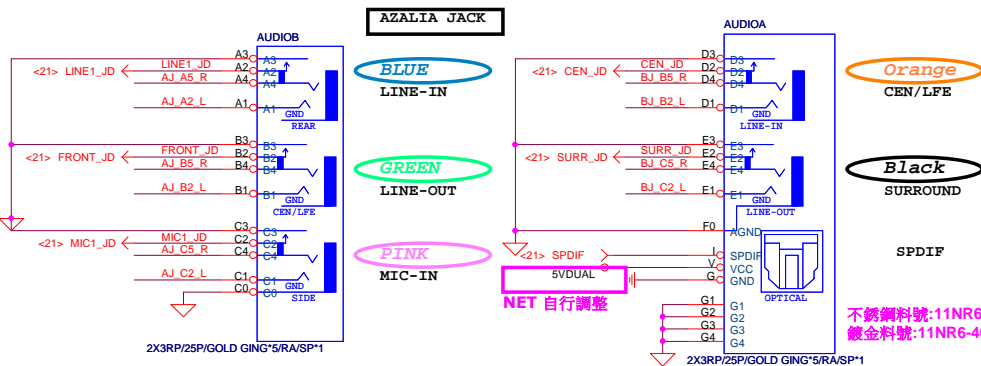
SURROUND



CEN/LFE

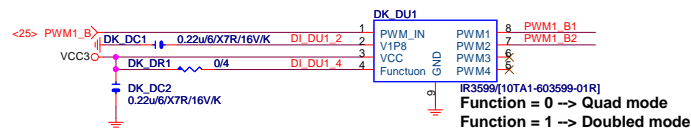
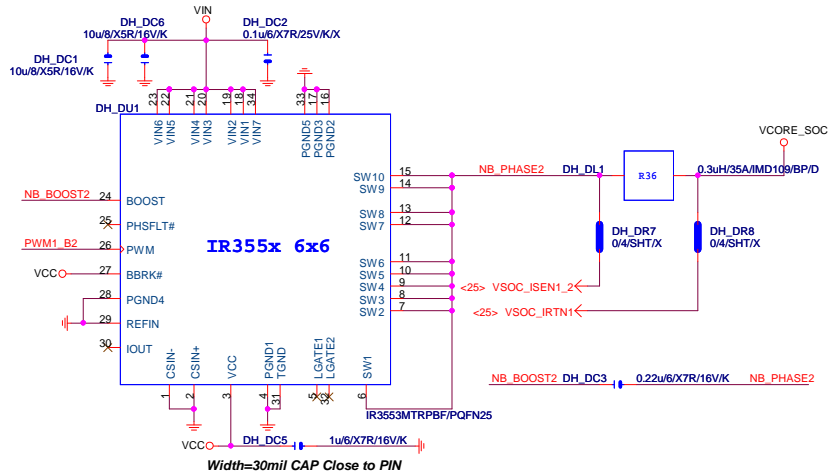
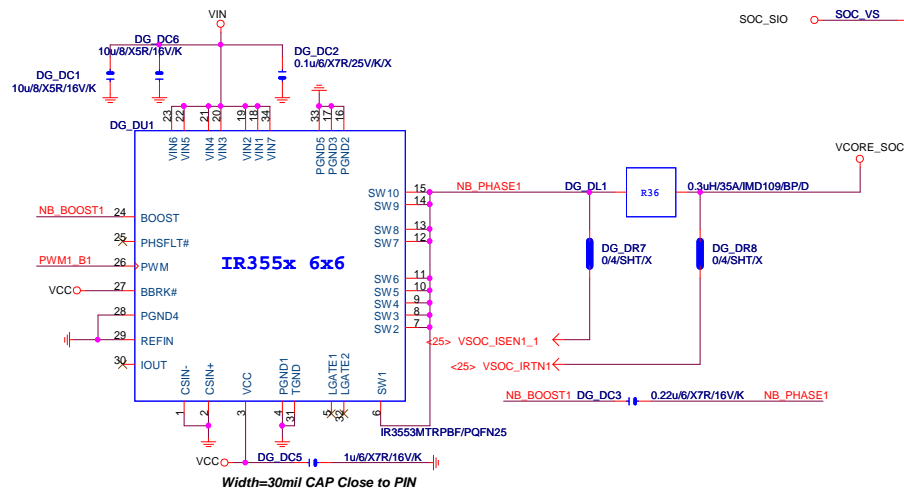


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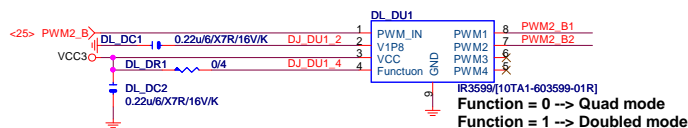
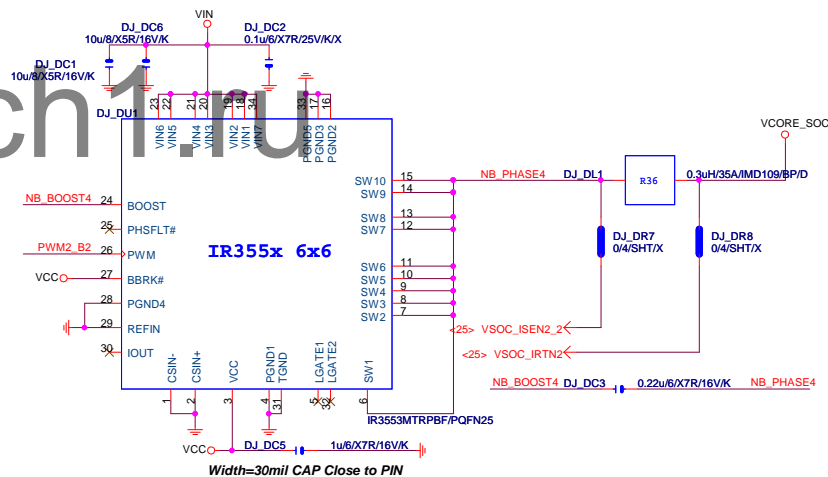
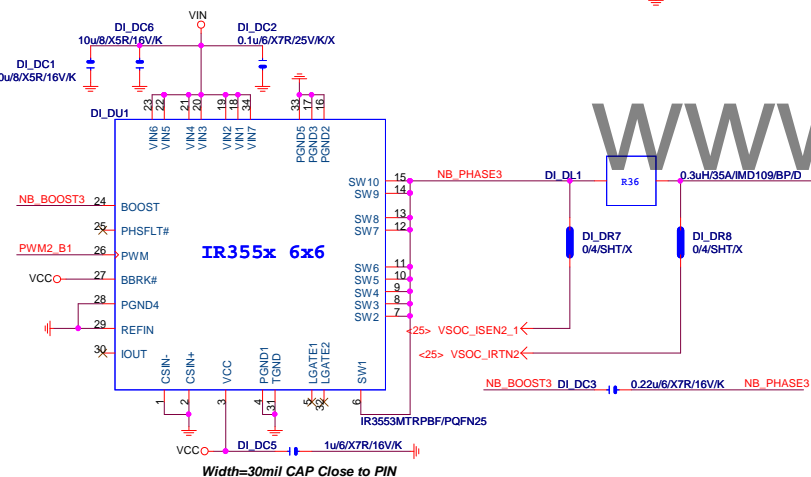




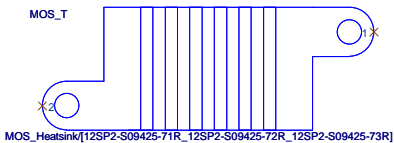
Vcore_Soc



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MOS HEATSINK

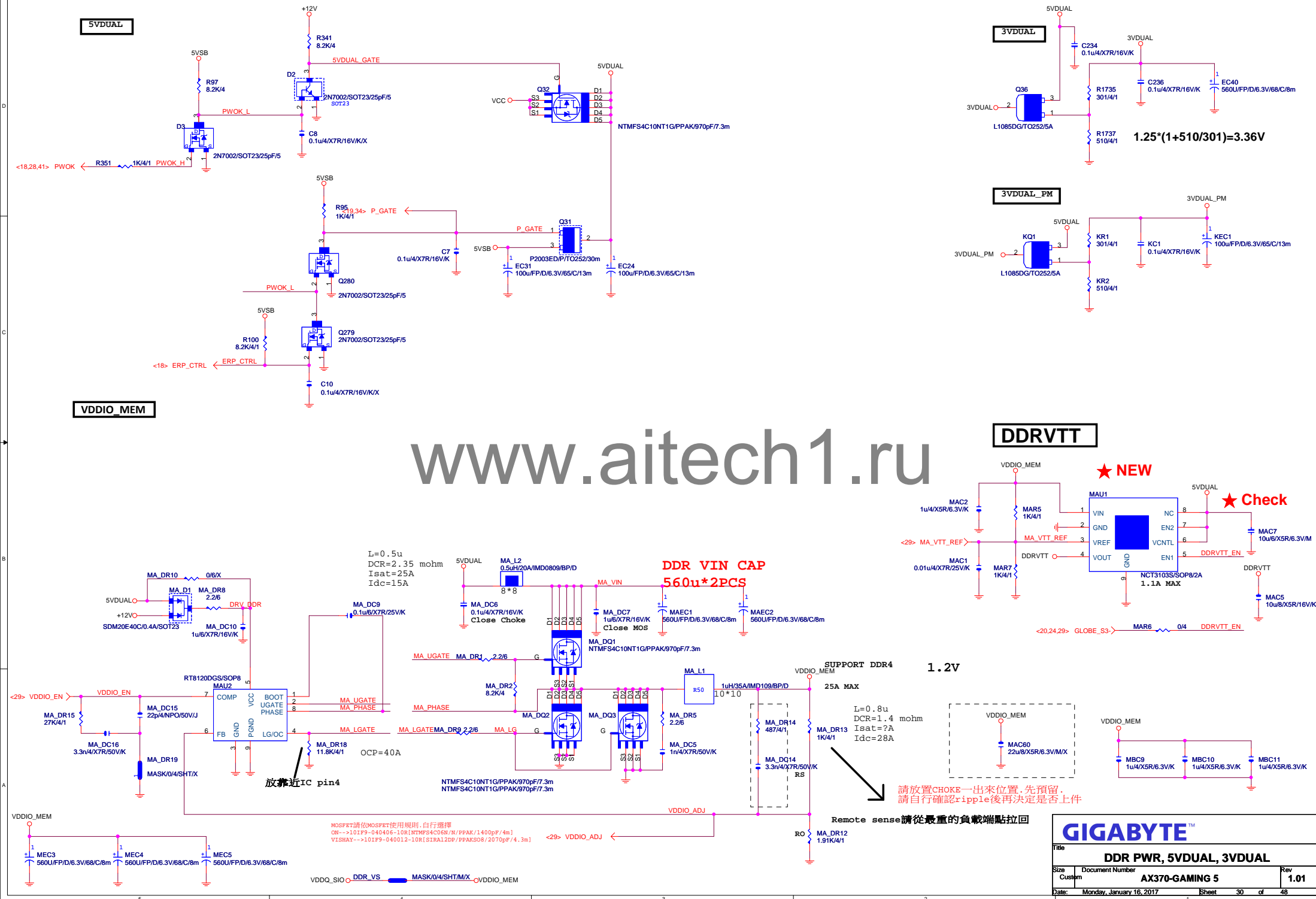
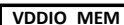


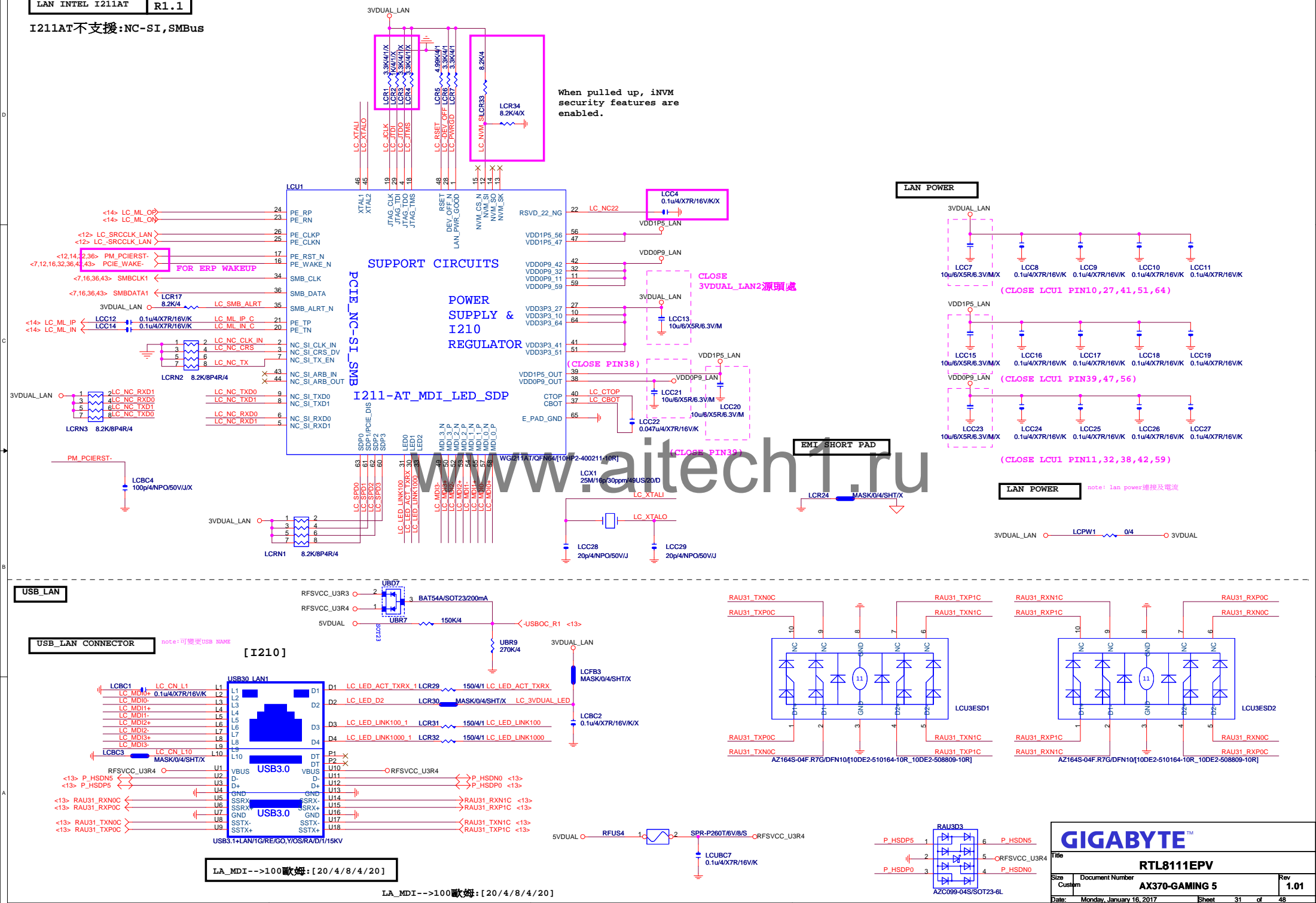
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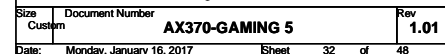
VCORE_SOC		
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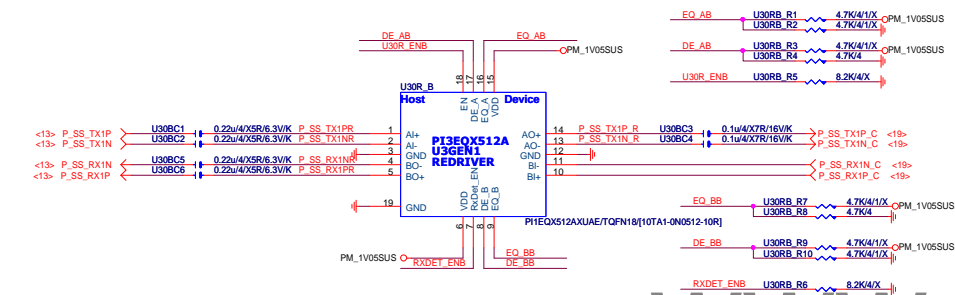
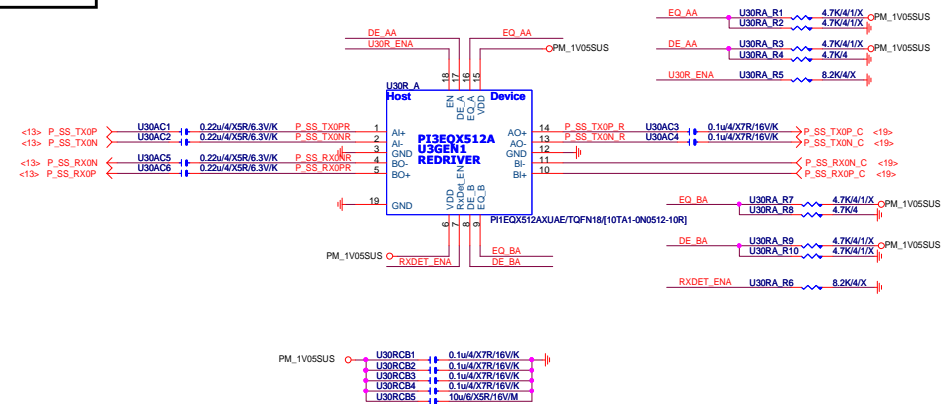
www.aitech1.ru



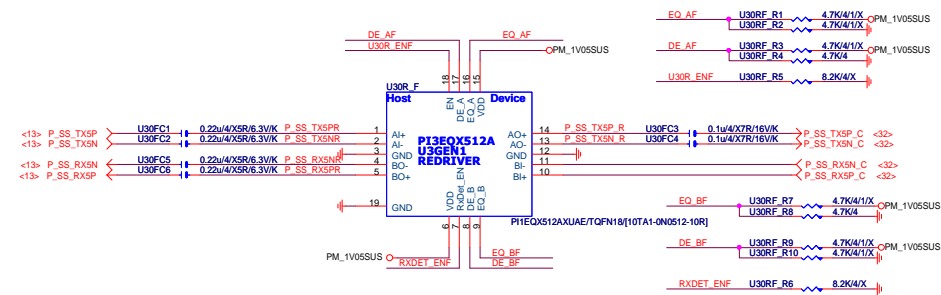
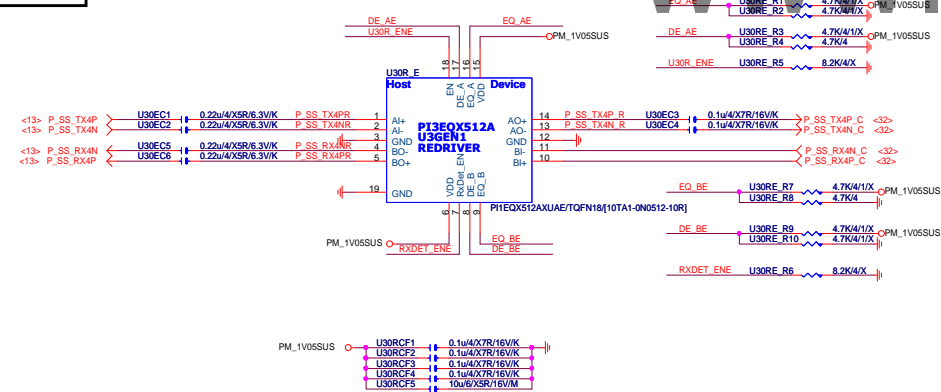




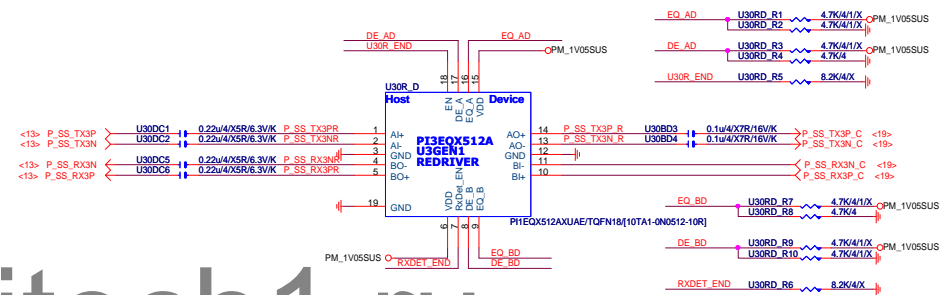
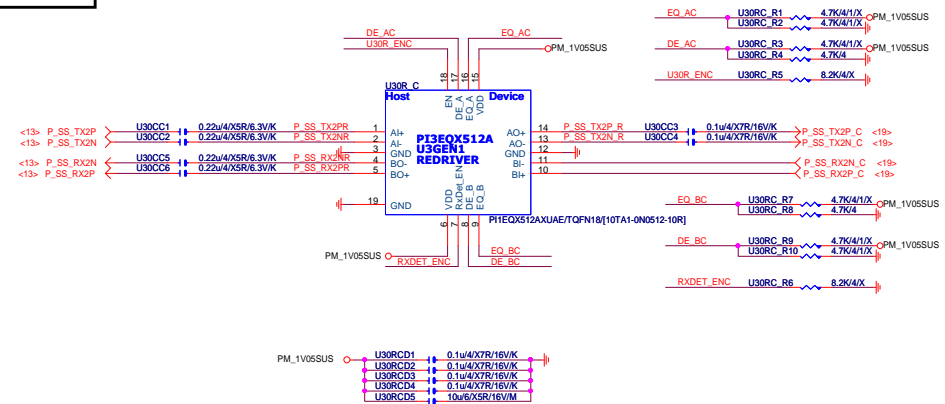
F_USB30_1



R_USB30

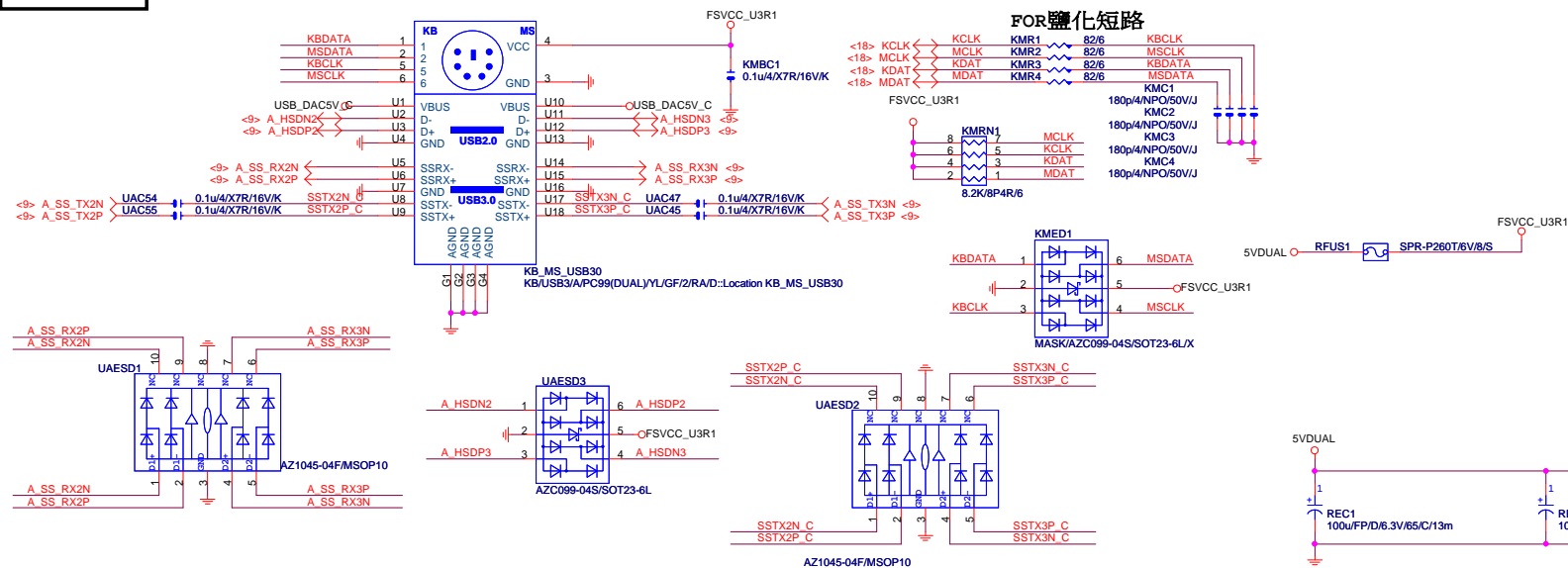


F_USB30_2



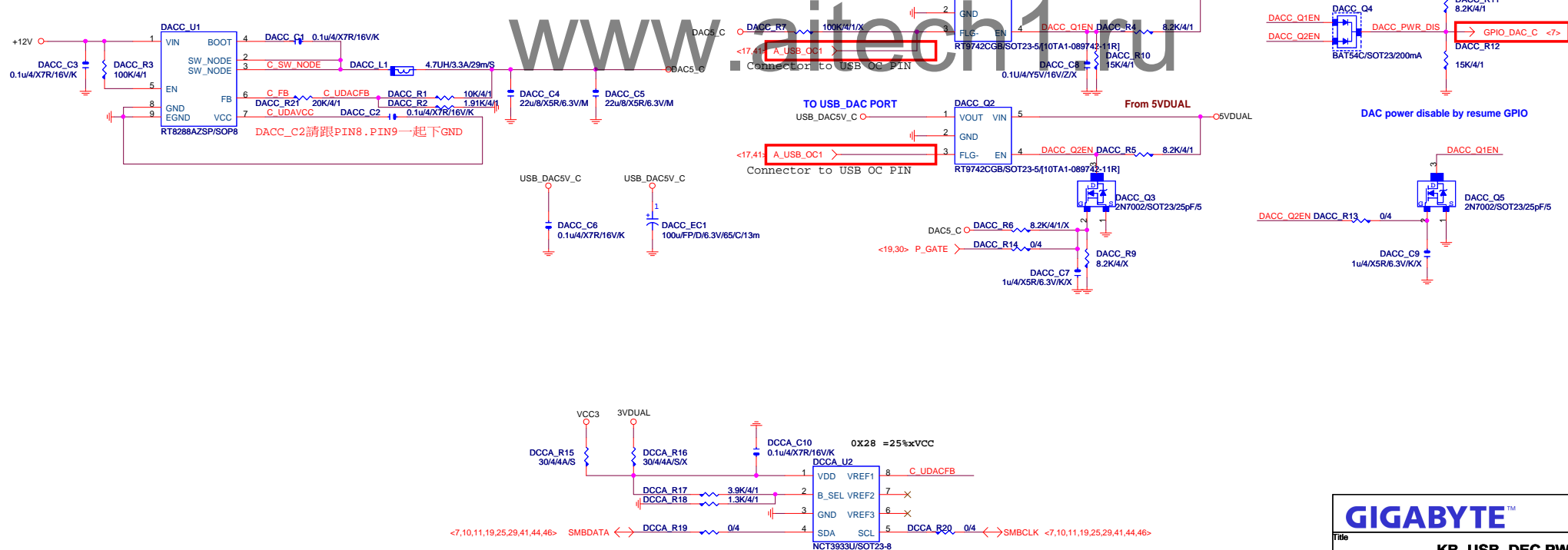
www.aitech1.ru

KB/MS/DAC PWR

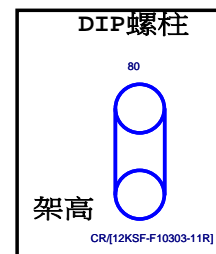
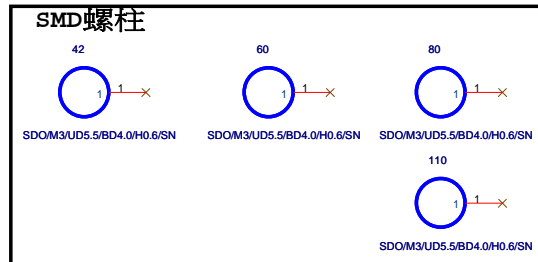
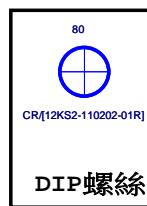
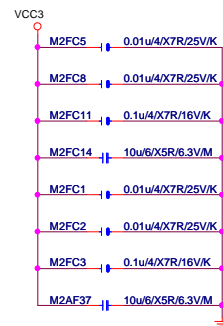
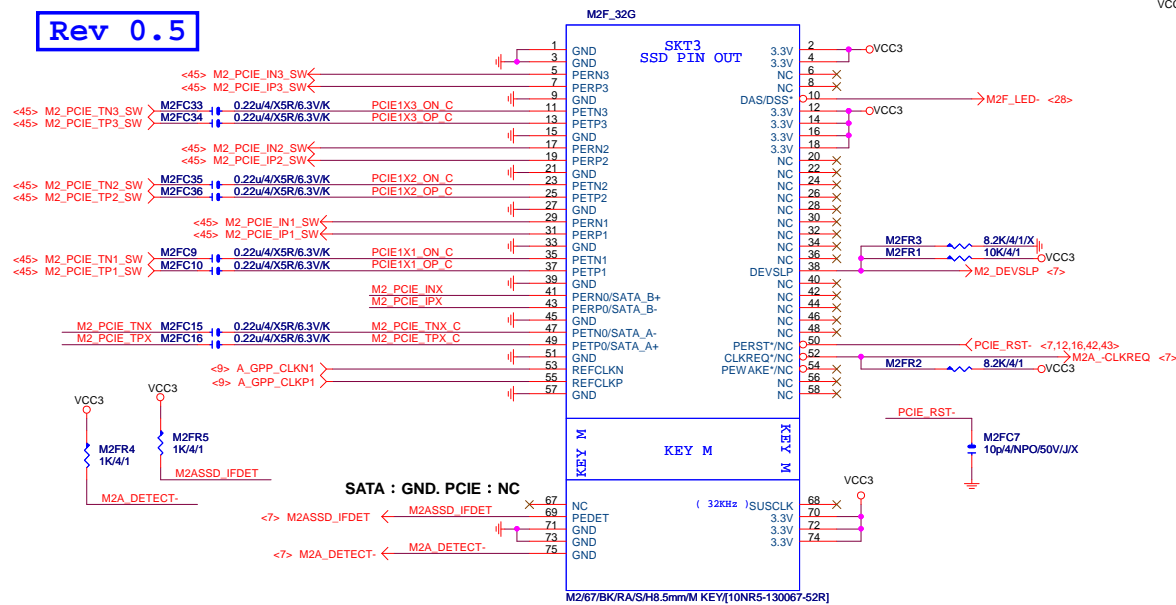


USB_DAC_C

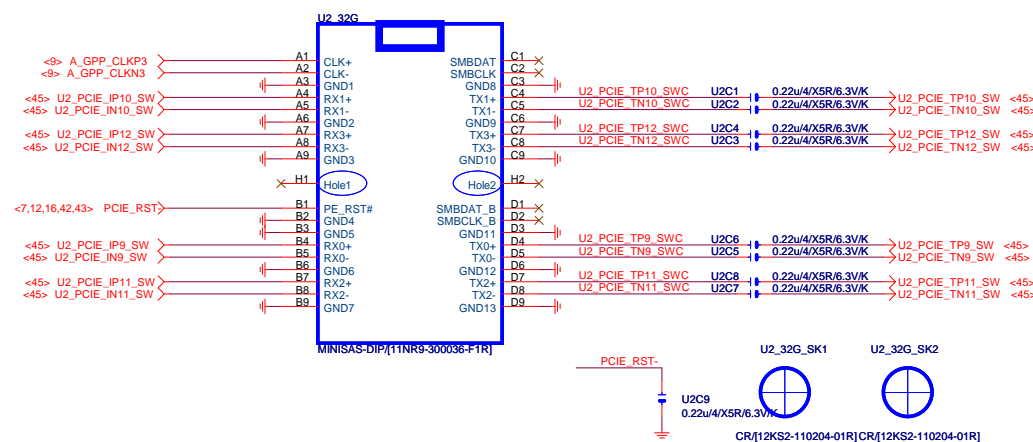
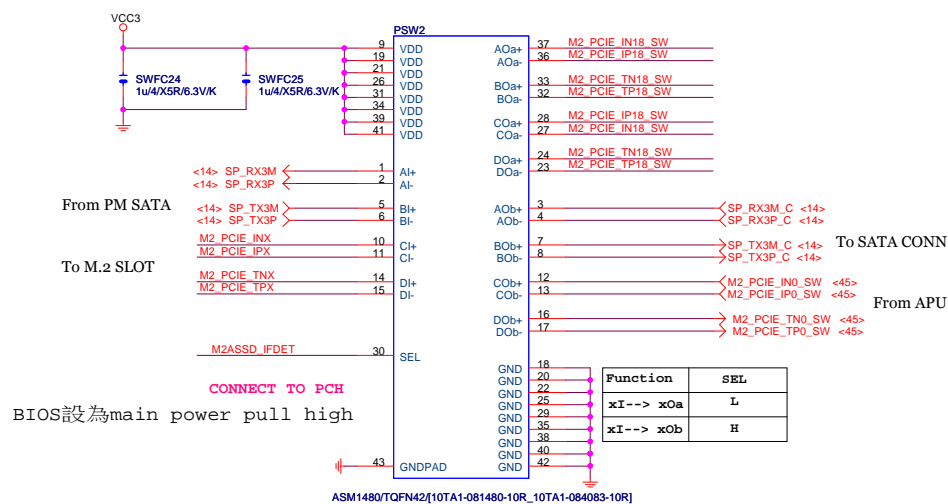
Rev0.12



Rev 0.5



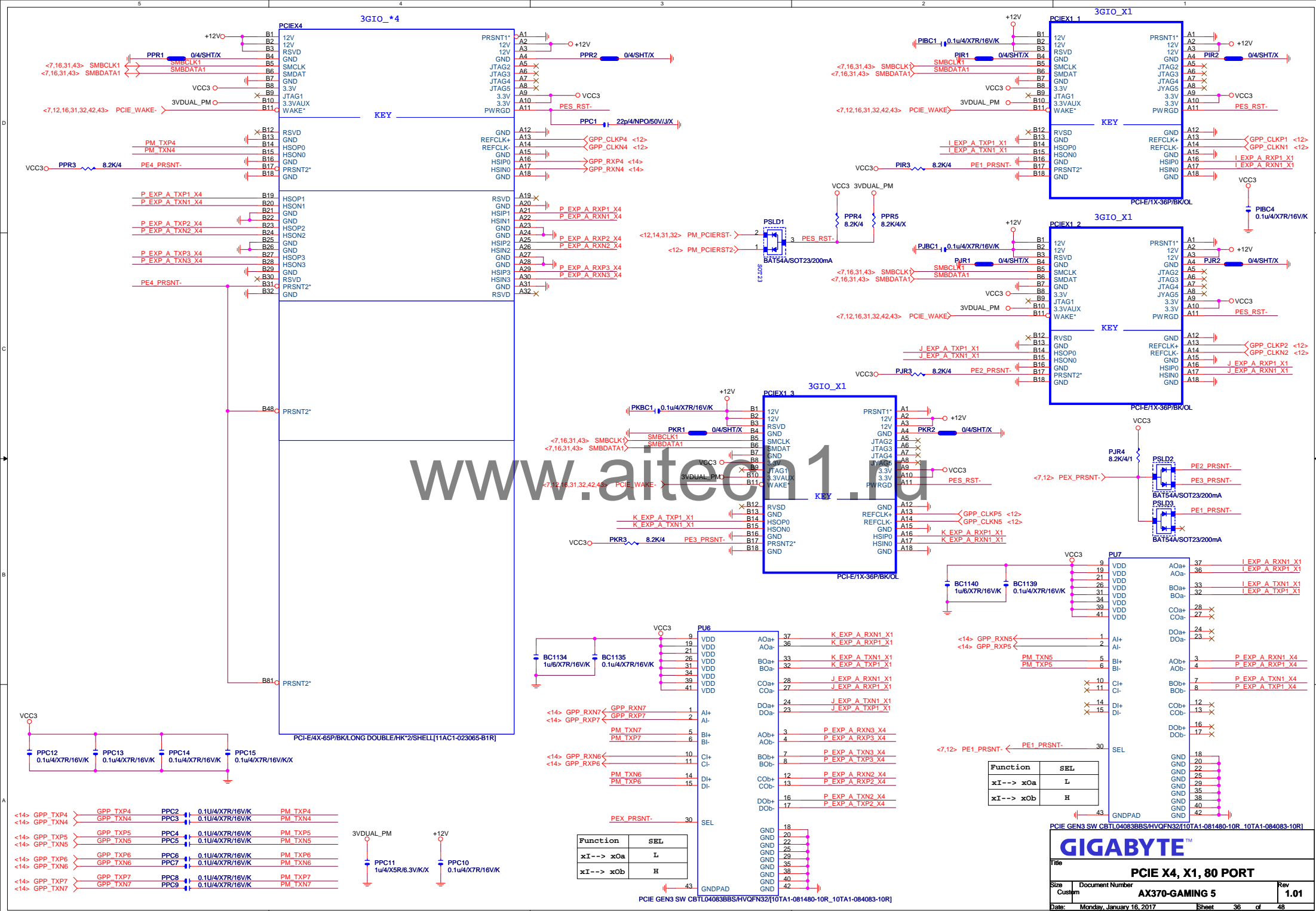
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GIGABYTE

Title	U.2, M.2 SOCKET
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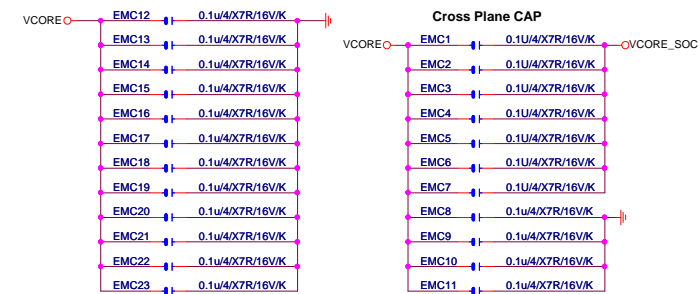
Size	Document Number	Rev
Custom	AX370-GAMING 5	1.01
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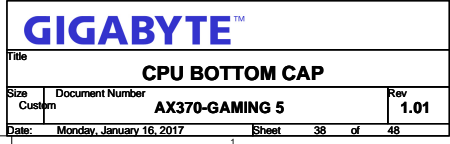


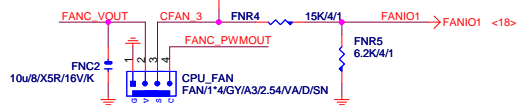
CPU TOP CAVITY



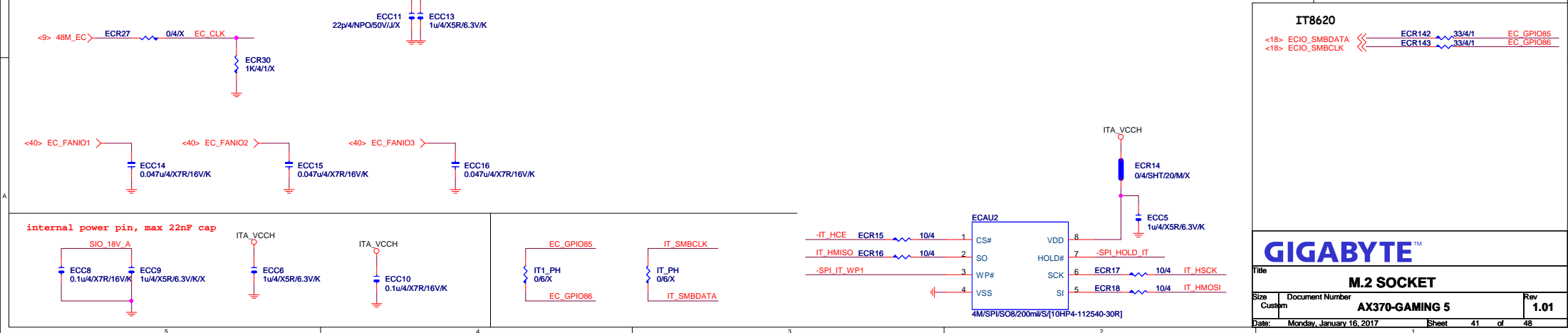
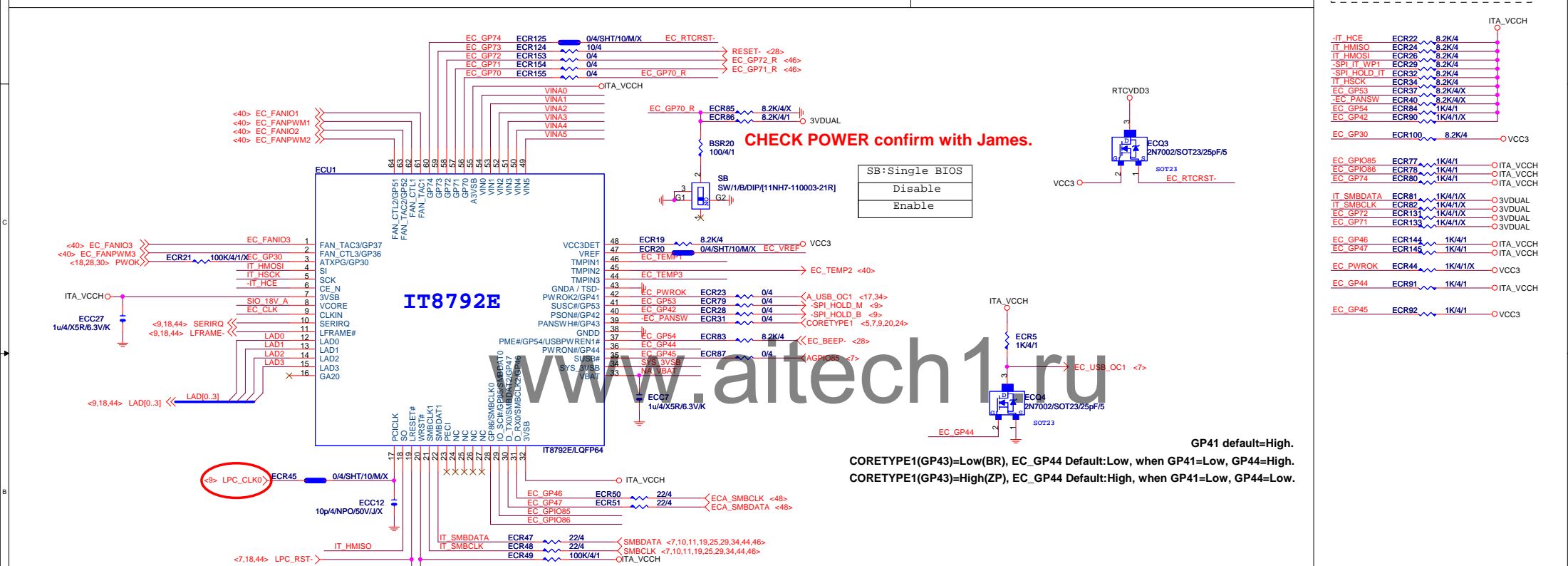
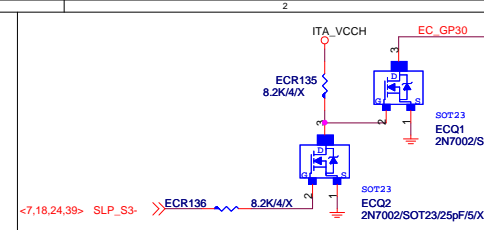
www.aitech1.ru





[illegible][illegible][illegible][illegible][illegible][illegible]

KBL FAN LOCATION MAP REFER TO PAGE.27

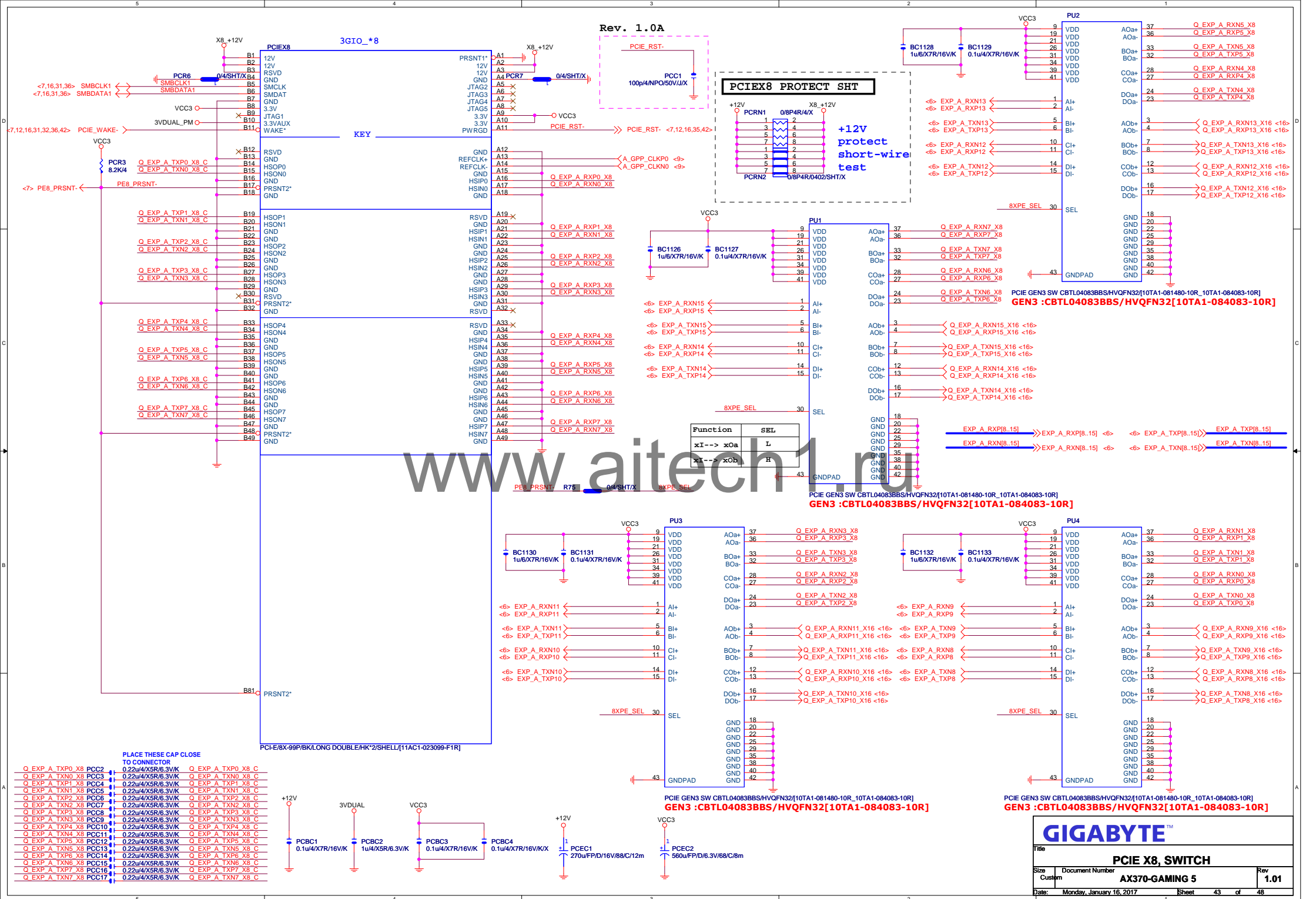


To PCIe host.

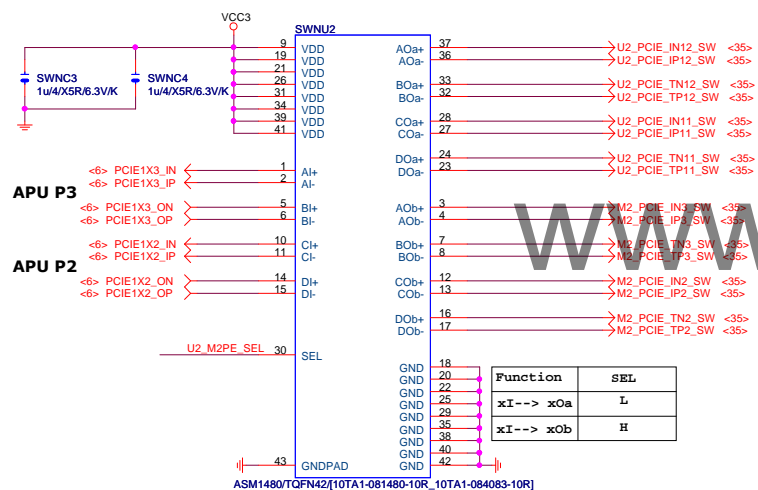
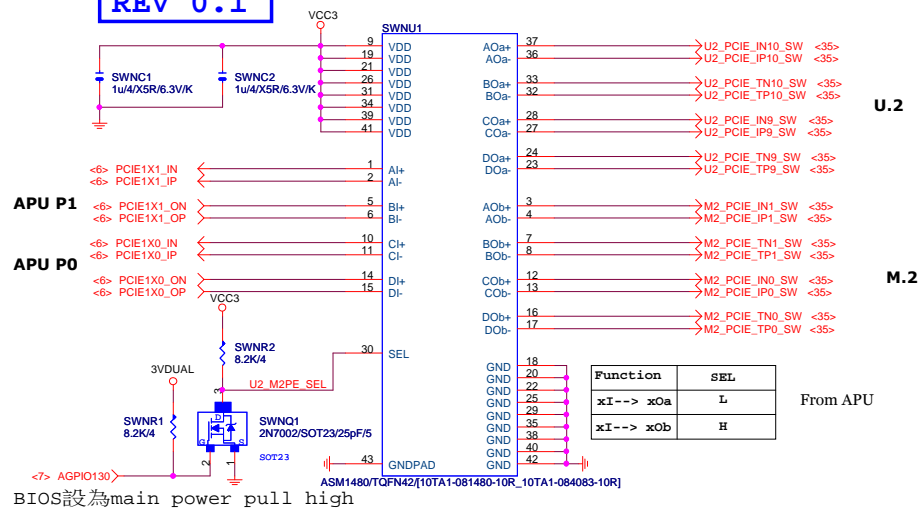
ASM1143 USB3.1

Base on ASM1142 0.3 Reference SCH





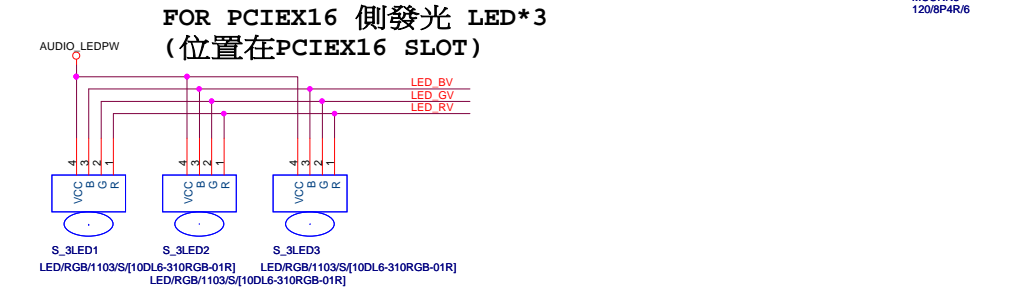
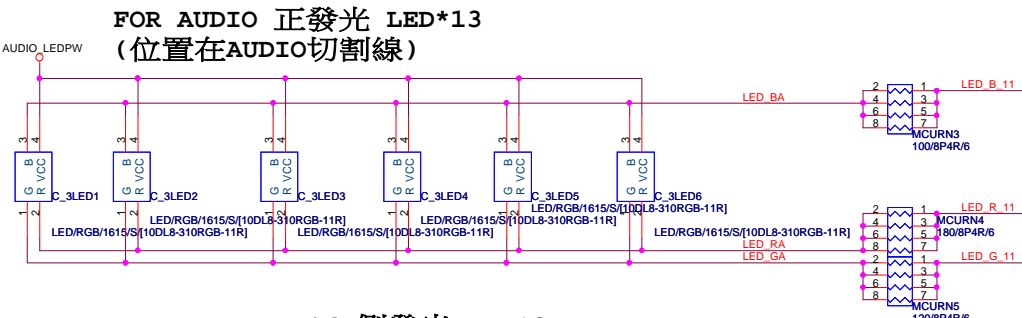
REV 0.1



→U2_PCIE_TP11_SW <35>
→M2_PCIE_IN3_SW <35>
→M2_PCIE_IP3_SW <35>
→M2_PCIE_TP3_SW <35>
→M2_PCIE_TP3_SW <35>

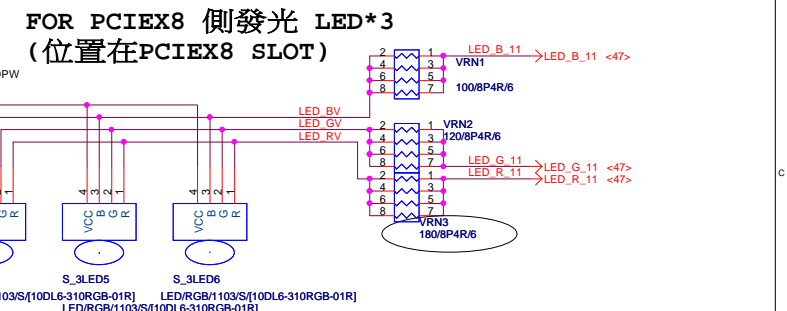
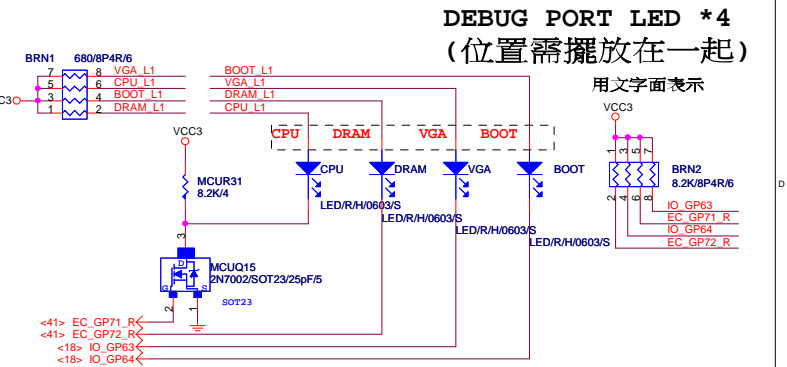
第一區 LED

Rev 0.63

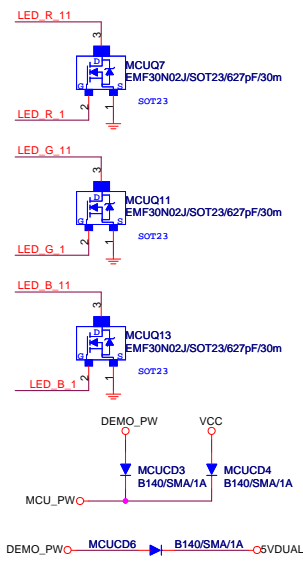


LED GPIO PIN DEFINE

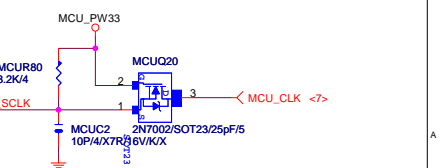
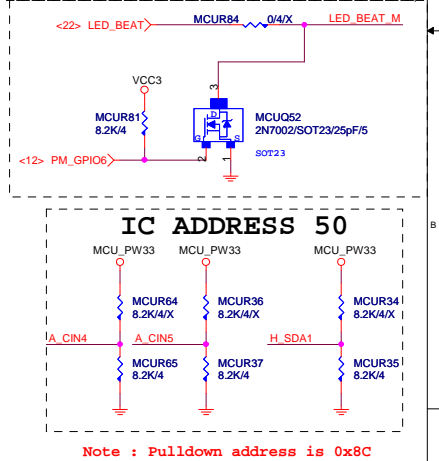
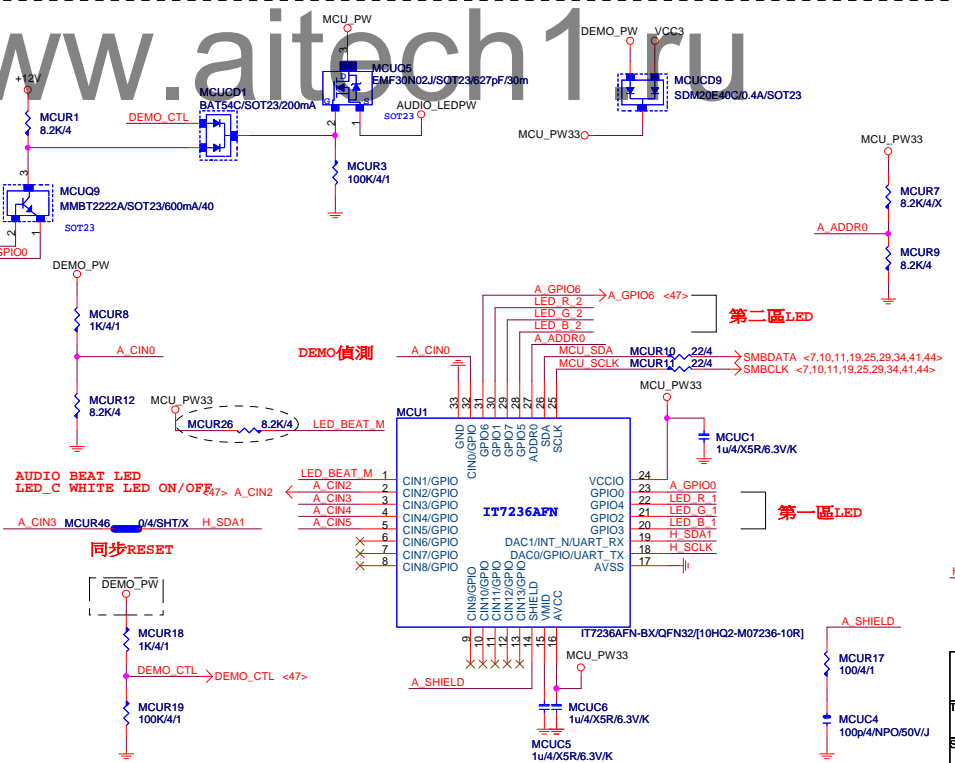
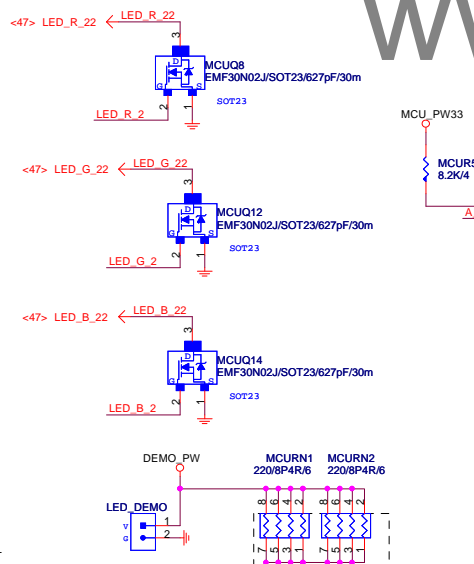
EC_GP71_R	CPU DEBUG
EC_GP72_R	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEBUG
PM_GPIO5	LED_C LED SWITCH
PM_GPIO6	PCIE16 LED SWITCH
PM_GPIO7	PCIE16 LED SWITCH



第一區 LED CONTROL



第二區 LED CONTROL



GIGABYTE

Title: CPU / AUDIO / PCIE/REAR LED

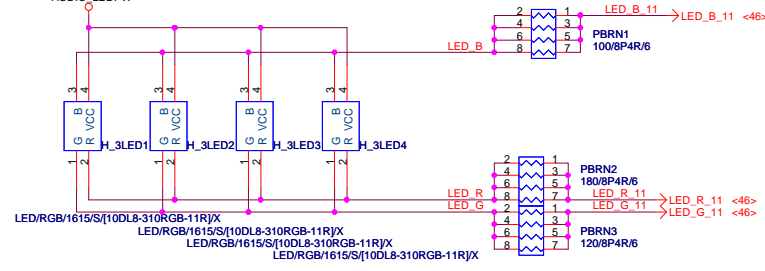
Size: Document Number AX370-GAMING 5

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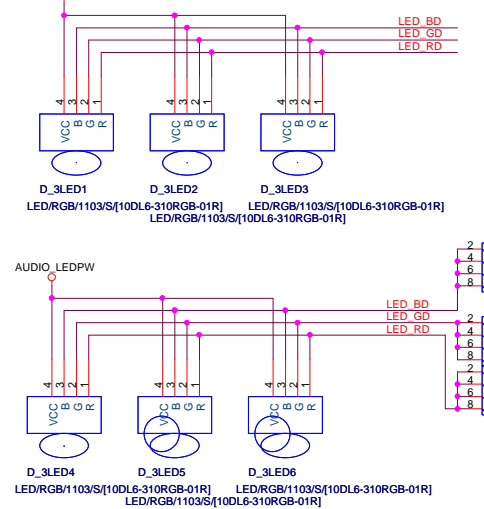
第二區 LED

Rev 0.63

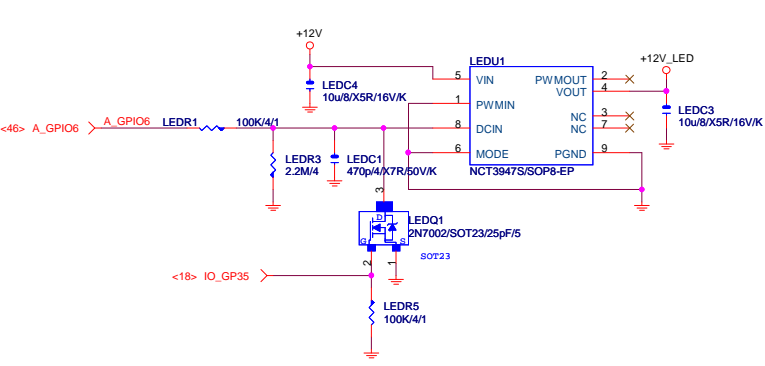
FOR PCH 正發光 LED*4 (依據PCH_HS設計擺放)



FOR DIMM 側發光 LED*6 (位置在DIMM兩側)



FOR 燈條 LED (LED_C放在PCB左邊板邊位置)



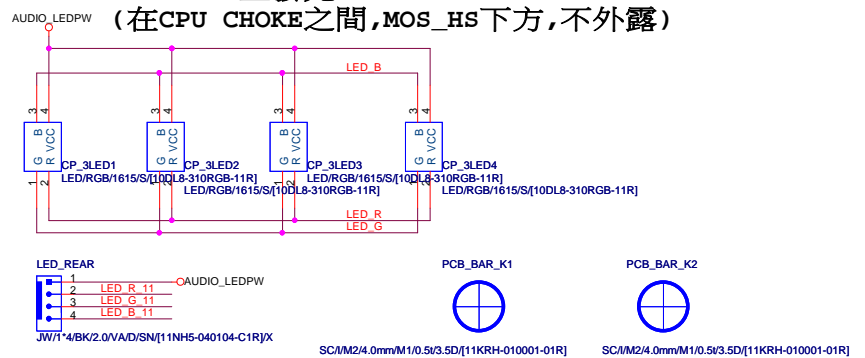
DDR燈條*3



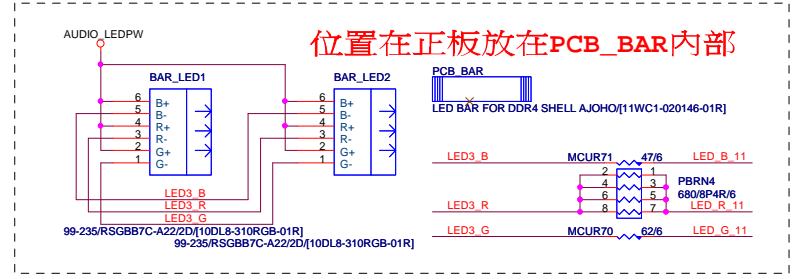
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MASK XPM AND TURBO??? FOOTPRINT

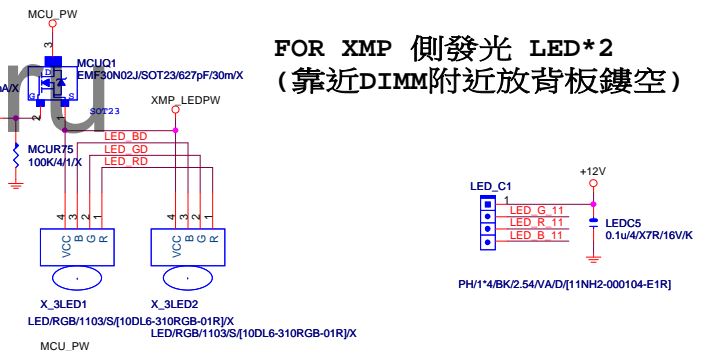
FOR CPU 正發光 LED*5 (在CPU CHOKE之間,MOS_HS下方,不外露)



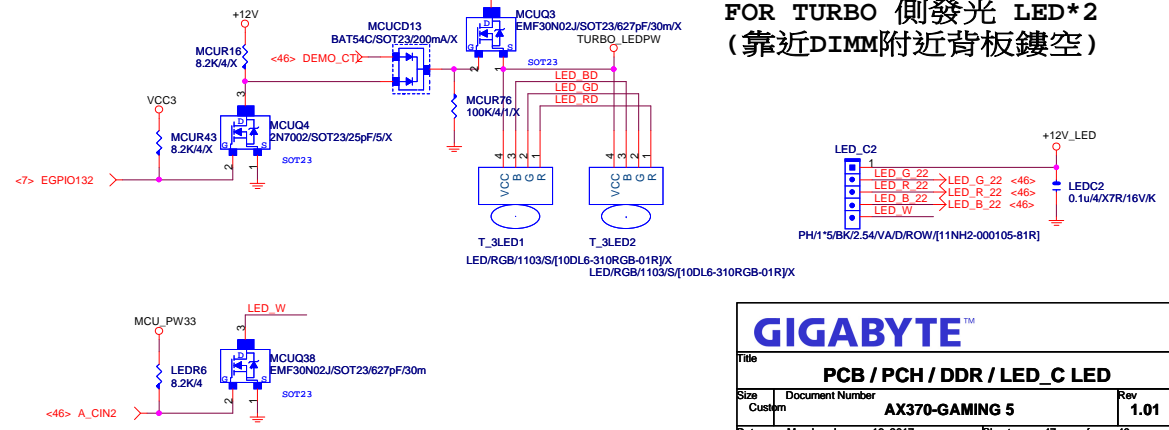
位置在正板放在PCB_BAR內部

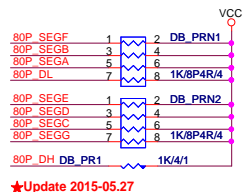
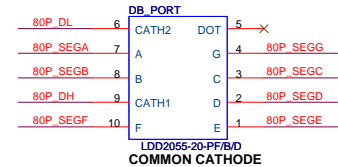
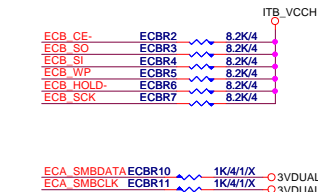
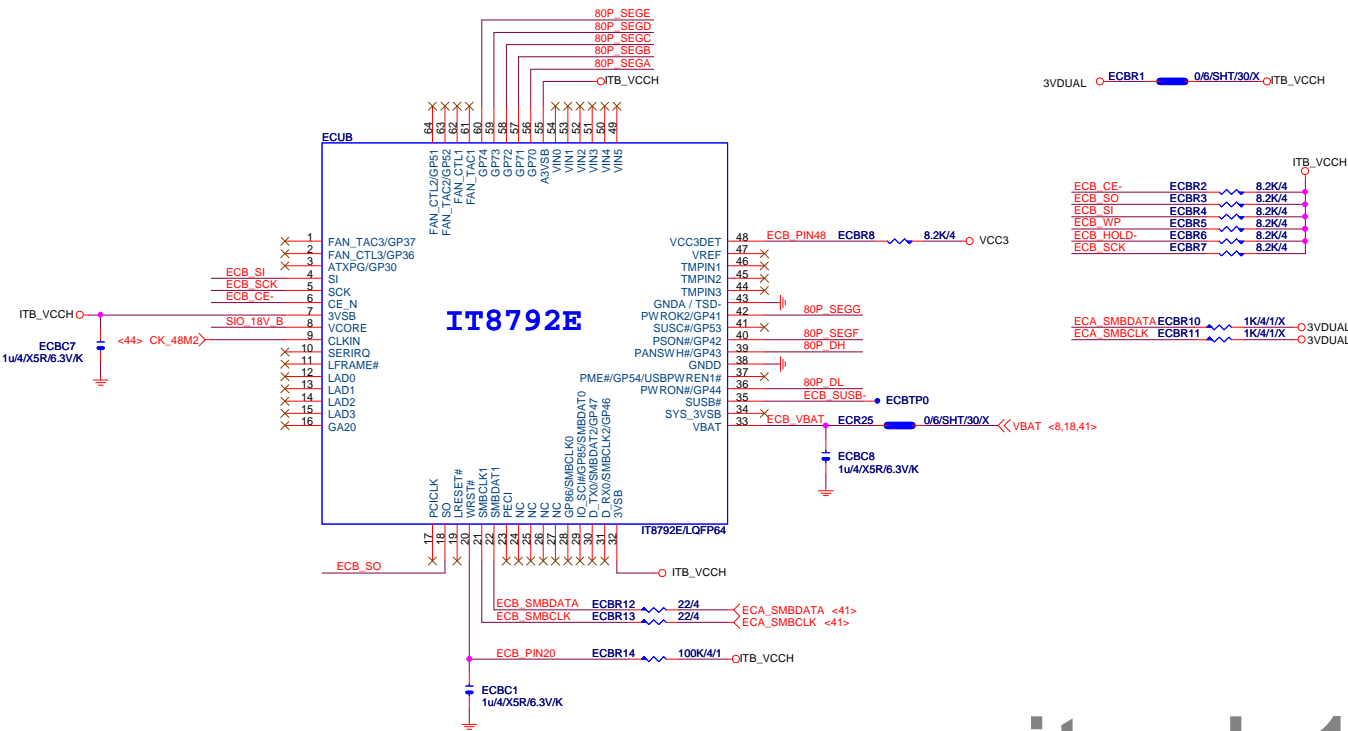


FOR XMP 側發光 LED*2 (靠近DIMM附近放背板鏤空)



FOR TURBO 側發光 LED*2 (靠近DIMM附近背板鏤空)





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